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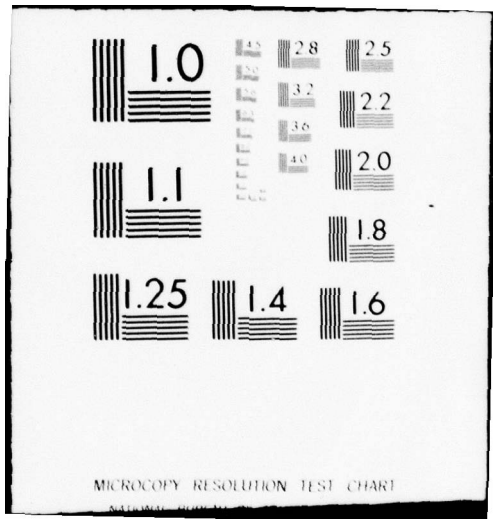
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LEVEL II

# HIGH SPEED A/D CONVERTERS SYSTEMS APPLICATIONS STUDY

## FINAL REPORT

2701

TRW NO. 31891
AUGUST 1978



Prepared for

NAVAL ELECTRONICS SYSTEMS COMMAND
Washington, D.C.
CONTRACT NO. N00039-78-C-0057



TRW
DEFENSE AND SPACE SYSTEMS GROUP

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## ABSTRACT

This report presents the results of a 6 month study of the Navy's present and future needs in high speed A/D converters, and the A/D converter technologies that have potential to fill those needs.

System requirements are examined in communications, radar, optical/IR, EW/ELINT, and sonar systems. Generic requirements and specific systems are discussed along with projections to future system high speed A/D converter needs.

Five A/D converter technologies, development requirements, and potential for satisfying the Navy's systems high speed A/D needs are examined. The technologies covered are: silicon bipolar, gallium arsenide FET, gallium arsenide TED/FET, Josephson junction, and electro-optical.

The report concludes with a summary of the Navy's present and future needs in high speed A/D converters, and the potential and developmental requirements of the five A/D technologies. Recommendations are made for developments of A/D converters using existing technology and A/D technology developments.

CONTENTS

CONTENTS (Continued)

# 1. INTRODUCTION

This report presents the results of a 6 month study of the Navy's present and future needs in high speed A/D converters, and the A/D converter technologies that have potential to fill those needs.

System requirements are examined in communications, radar, optical/IR, EW/ELINT, and sonar systems. Generic requirements and specific systems are discussed along with projections to future system high speed A/D converter needs.

Five A/D converter technologies, development requirements, and potential for satisfying the Navy's systems high speed A/D needs are examined. The technologies covered are: silicon bipolar, gallium arsenide (GaAs) FET, gallium arsenide TED/FET, Josephson junction, and electro-optical.

The report concludes with a summary of the Navy's present and future needs in high speed A/D converters, and the potential and developmental requirements of the five A/D technologies. Recommendations are made for developments of A/D converters using existing technology and A/D technology developments.

Silicon bipolar is the recommended technology for A/D converter developments using existing technology. The large scale integration (LSI) capabilities of this technology have been employed for high speed A/D converter fabrication for over 4 years, resulting in the development of eight or more single chip silicon monolithic high speed A/D quantizers. The capabilities of this proven technology have not yet been fully realized. After examining the Navy's needs for high speed A/D converters, three single chip monolithic A/D converter developments are recommended:

- 5 Msps 12 bit
- 50 Msps 10 bit
- 250 Msps 6 bit (8 bit in 4 chip configuration).

These converters will satisfy all of the Navy's near term high speed A/D requirements for sampling rates up to 250 Msps. Each A/D, including a thin film hybrid sample and hold circuit, would require approximately 18 months to fully develop. Upon completion of AFAL Contract F33615-78-C-1428

for high speed monolithic sample and hold circuits, the potential will exist to combine a monolithic S/H circuit with each LSI quantizer to produce single chip monolithic A/D converters.

Gallium arsenide FET is the recommended technology to be developed for advanced A/D converter developments. This technology offers at least an order of magnitude speed • power advantage over silicon. Nearly all of the Navy's needs for high speed A/D converters can be met with only two GaAs A/Ds:

- 50 Msps 12 bit
- 1000 Msps 6 or 8 bit.

Both of these A/Ds can be developed as single chip monolithic converters including the S/H. Gallium arsenide is a developing technology that has received increasing attention in both government and industry. Some small scale integrated circuits have already been developed and processing yields are continuing to improve. LSI levels of integration are only a few years off. A recommended GaAs technology development program is described in Section 4 of this report.

# 2. SYSTEM REQUIREMENTS STUDY

As Naval warfare has become increasingly sophisticated, so have the requirements on electronic systems. Those systems which process and/or provide information have literally exploded in their necessity for speed, accuracy, and sophistication. Systems which traditionally use analog components have evolved to digital implementations to achieve higher reliability and accuracy at greater speed and at resonable costs. Once the signals in an electronic systems are represented digitally, many opportunities are opened for storage, processing, and communication. This section addresses applications of A/D converters to Naval systems. Some examples of communications, radar, optical/IR, electronic warfare and sonar systems, including their organization and A/D requirements, are presented.

## 2.1 COMMUNICATION SYSTEMS

An important trend in communication systems has been the replacement of analog by digital hardware from the baseband data processing into IF and in some cases RF sections.

Digital implementations offer several benefits including improved accuracy, greater dynamic range, and better stability. These factors are particularly important in the design of antijam (AJ) communication systems such as in the acquisition and tracking of synchronization. Auxiliary data functions such as error correction coding/decoding, and data compression (video or voice) rely almost entirely upon digital implementation.

A/D converters are used extensively in today's communication systems. Typical applications are: secured communications (antijam, encryption), digital receivers, and bit synchronizers. The following sections detail some of the communication systems and their A/D requirements.

### 2.1.1 Secured Communications Systems

In these systems, digital baseband signals are multiplied by direct PN sequences of a much higher rate than the data to provide secure or antijamming communications. The received signal is A/D converted and correlated (directly or by FHT) to remove the direct PN coding and restore the data. Sampling in the transmitter is performed based on the data rate with a

number of bits sufficient to provide a low reconstruction error. Sampling at the receiver is performed at least as fast as the PN chip rate, and often I-Q sampling is performed.

Frequency hopping is another spread spectrum technique utilized in anitjam communications whereby the transmitting frequency is randomly changed at a rapid rate making interception very difficult. Spread spectrum receivers require sophisticated synchronization acquisition and tracking circuits which require digital implementation.

### 2.1.2 Digital Receivers

The objective of a digital receiver is to digitize the analog information from the antenna as soon as possible so that digital processing flexibility can be utilized. This implies that the sampling (via an A/D converter) can be done either on some IF frequency or at baseband. Whereas many other applications require high speed A/D converters, the HF receiver requires high dynamic range (large number of bits), and good IM performance. A block diagram for a typical HF receiver is shown in Figure 2-1. It is seen that A/D conversion takes place at the final IF frequency. Frequency translation to baseband is performed by the sampling process in the A/D converter. Demodulation is carried out in a processor which offers the flexibility to detect any one of a number of different signal designs. One of the requirements for this type of receiver is the intermodulation (IM) requirement. IMs are required to be 60 to 80 dB below large adjacent signals to avoid degradation for small signals. This implies 7 to 10 bits for an ideal converter since IMs follow a 9N law (9 dB per bit) for a single tone.

### 2.1.3 Bit Synchronizers

All digital communication systems require a bit synchronizer in the receiver. Traditionally, bit synchronizers have been designed for uncoded systems and have operated at reasonably high SNRs of 7 dB or higher. Advanced systems are requiring higher data rates, coded data, and operation at low SNRs. The traditional analog bit synchronizer cannot achieve good performance in these systems. A digital bit synchronizer offers improved performance (0.5 to 1 dB from theory), a high degree of producibility, and

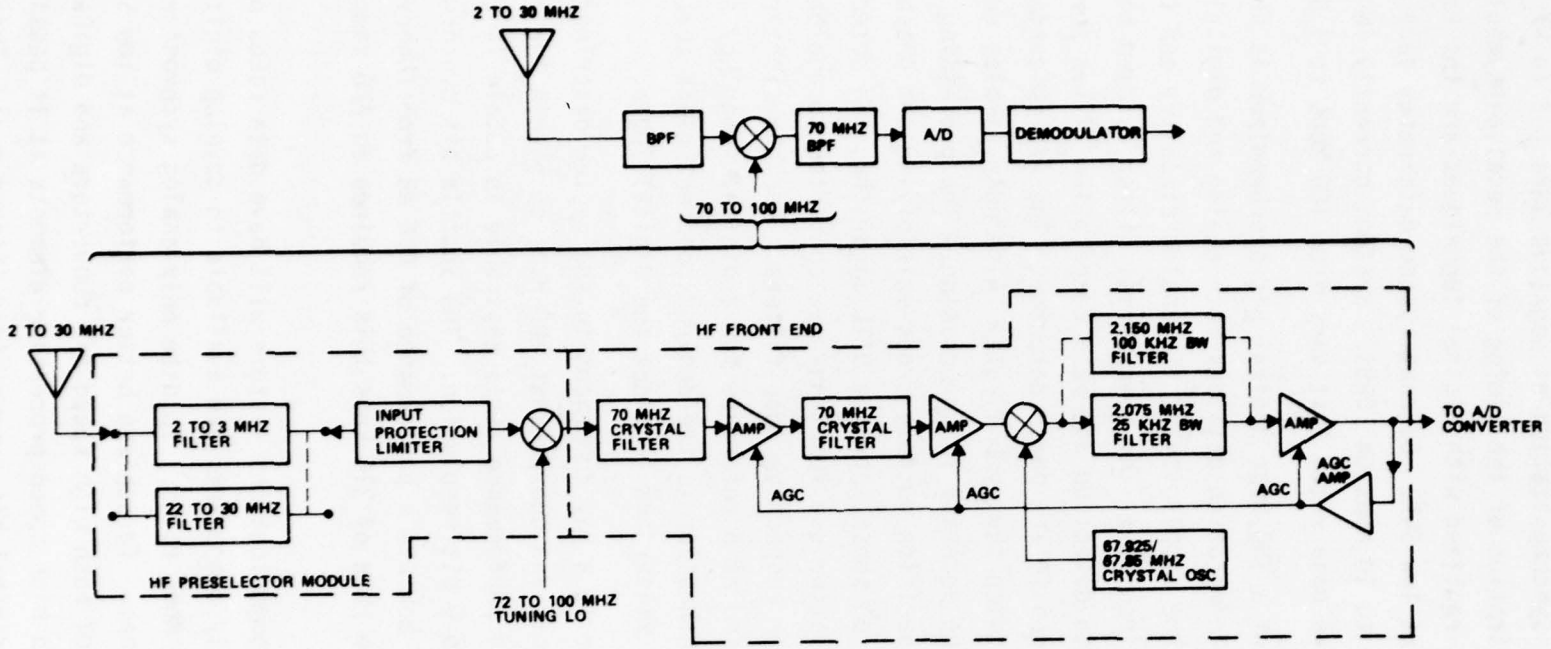



Figure 2-1. Narrowband Receiver Design

parameter stability. Synchronization at negative SNRs (-2 to -7 dB) requires accurate estimation of the timing of the received symbols. The low processing errors realized with digital techniques are the key to successful operation at low SNR. Current system data rates vary from 200 kbps on space shuttle to 10 Mbps on TDRSS. Systems currently in the early development stages have data rates that vary from 100 Mbps to 1 Gbps.

A block diagram of a 100 Msps digital bit synchronizer is shown in Figure 2-2. This implementation utilizes both analog and digital circuitry to take advantage of the simplicity of the analog circuitry and the precision of the digital circuitry. The transversal filter is used both as matched filter for data detection and as a correlation filter for the data transition tracking loop (DTTL) phase detector. The A/D converter samples the filter output at twice the symbol rate. Alternate samples go to the data detector and phase detector for processing. The processing consists of encoding the soft decision output, cross-multiplying the phase error with the data transition sense, per the DTTL algorithm, and detecting the baseline error. The latter two functions are converted to analog signals for processing by their respective loop filters. For the clock recovery loop, and LC VCO is used as a reference for a digital frequency synthesizer. The output of this synthesizer is the desired coherent clock that is used to sample the matched filter and to clock the digital logic.

The A/D converter is a key component in the system described above. This A/D is a 4 bit unit and operates at 200 Msps to obtain two samples per bit. For improved performance it is desirable to obtain 16 to 32 samples per bit with 4 to 6 bit resolution. The shuttle bit synchronizer uses 32 samples per bit to achieve a performance of 0.6 dB from theory at an SNR of -5 dB. With sample rate of 216 kbps this requires an A/D sample rate of 6.4 Msps.

Future digital communications systems will have data rates of 100 Msps to a 1 Gbps. Currently components are available to develop digital bit synchronizers for 100 Mbps rates. To date only analog sychronizers are practical above 100 Mbps. To achieve better performance at low SNRs requires development of both high speed A/D converters and digital processing components. With high speed processing elements it is possible to develop a completely digital bit synchronizer (Figure 2-3). This would provide significant cost and performance advantages for future systems.

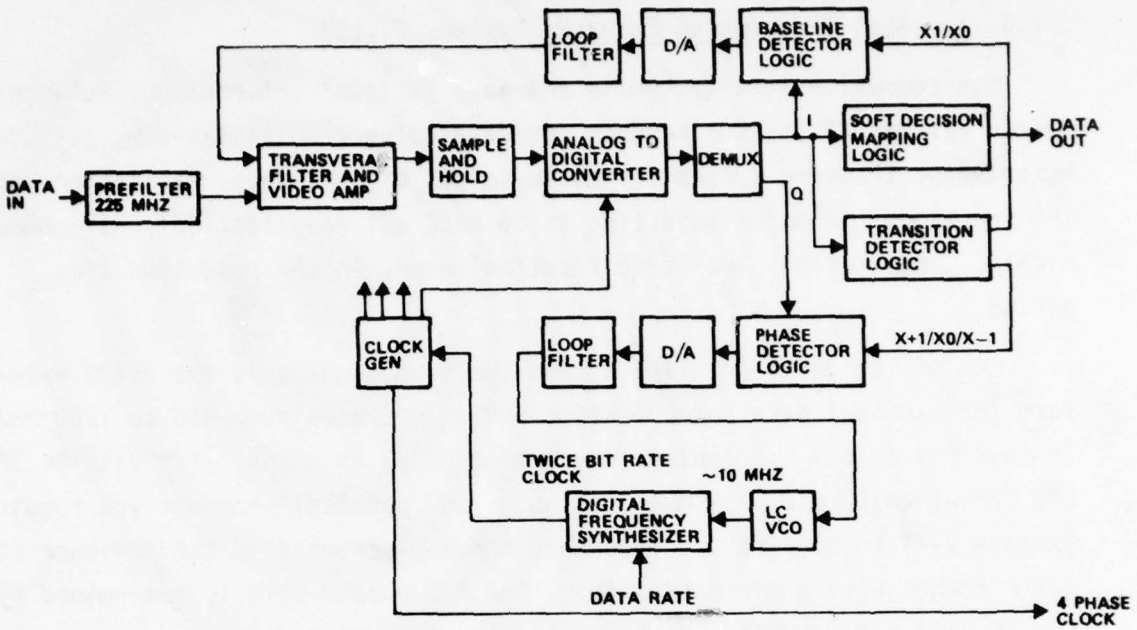



Figure 2-2. 100 Msps Symbol Synchronizer Block Diagram

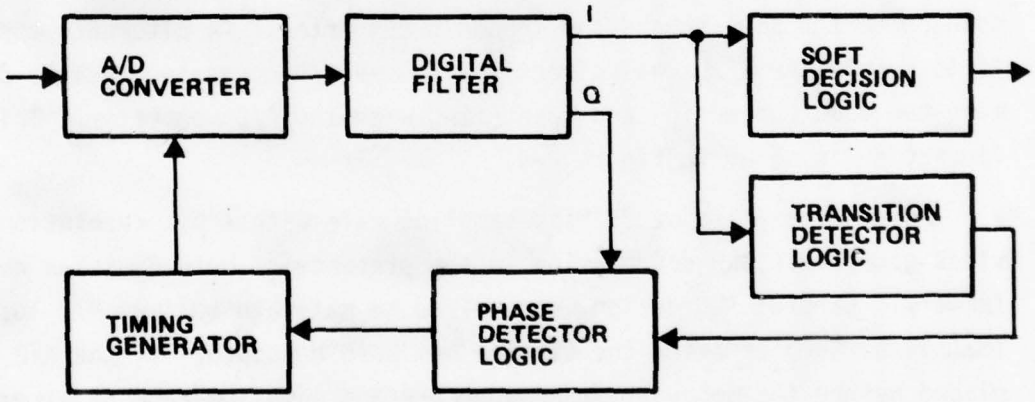



Figure 2-3. Fully Digital Bit Synchronizer

### 2.1.4 Tactical Information Exchange Systems (TIES)

One communications system is the Navy Tactical Information Exchange System (TIES). TIES is a program for developing a multiplatform, tactical information transfer system to handle voice, digital data, navigation, and IFF functions. A major objective is to meet all Navy tactical CNI (communication, navigation, and identification) needs in the post-1980 time period.

One of the pertinent TIES spread-spectrum signals is the JTIDS waveform for tactical data communications which operates from 960 to 1260 MHz. It consists of 6.4 sec pulses consisting of 32 PN chips. The data is 32-ary PPM at chip rate of 5 Mbps. A number of parallel channels are required (Figure 2-4) to acquire the frequency hopping preamble in the presence of interference with good sensitivity. The A/D sample rate is determined by the PN chip rate. Multiple chip rate operation is permitted by performing digital PN correlations, thus giving the receiver a multifunction capability. Each A/D converter operates on a dehopped, band limited segment of the wideband IF signal from the receiver. As originally conceived the IF signal is down converted to baseband and then A/D converted. An alternate approach is to sample the IF signal directly with the A/D converter thereby performing the down conversion and quantizing with the A/D converter. This configuration is shown in Figure 2-4.

An A/D operating at 25 Msps sampling rate with 4 bit resolution provides acceptable SNR degradation in the presence of both Gaussian and CW jammers. Careful AGC design is required to maintain optimum A/D loading. The system samples after the carrier has been dehopped. If the A/D were placed before the dehopper, then aperture and sampling rate requirements would dominate and the A/D design would be well beyond the present state of the art.

### 2.1.5 FLTSATCOM

A second Navy communications system with potential for using high speed A/D converters is the Fleet Satellite Communication System (FLTSATCOM). The FLTSATCOM system will provide the backbone Navy communucations capability in

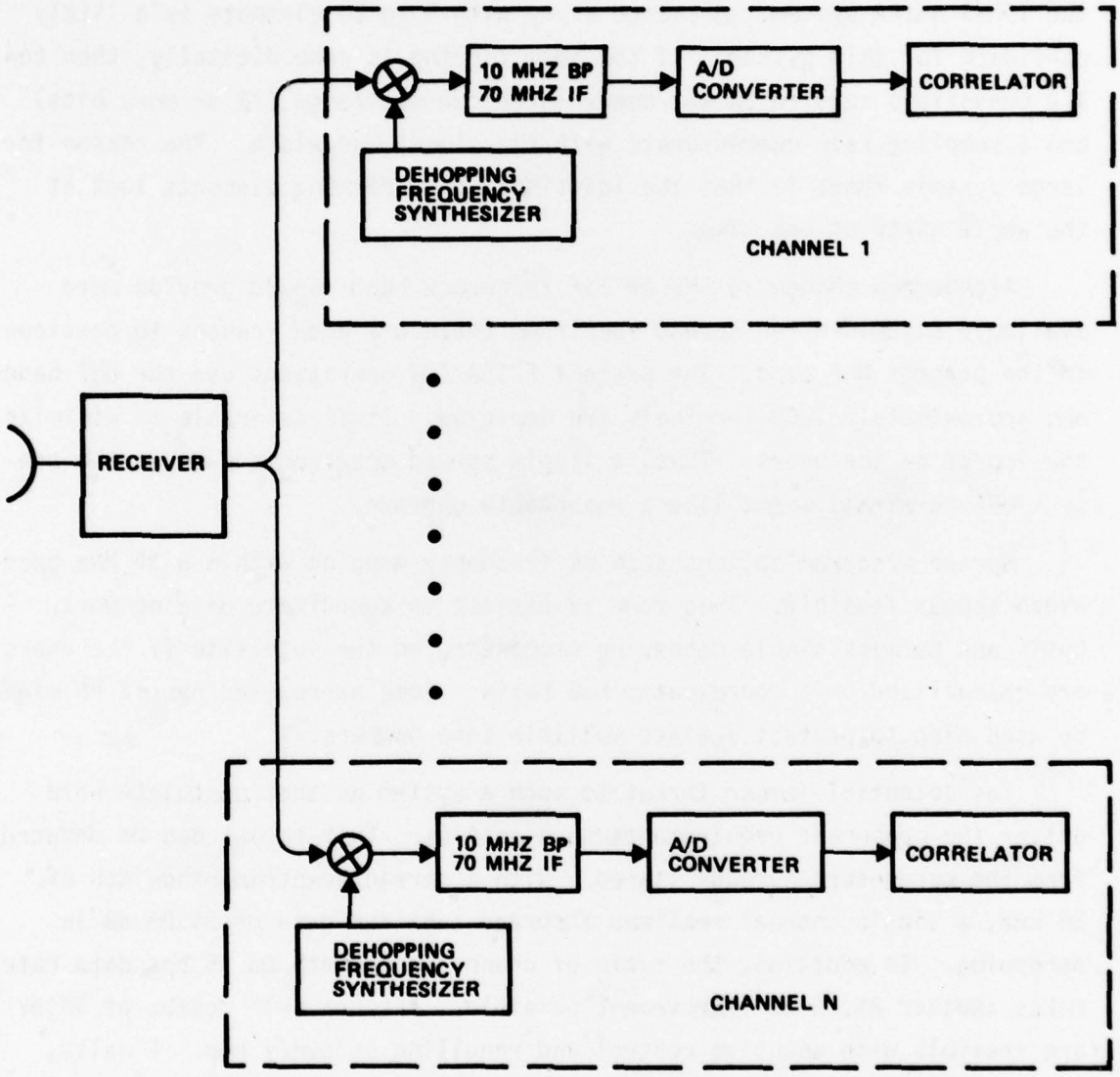



Figure 2-4. TIES Spread Spectrum Receiver and PN Demodulator

the 1980's and advance systems of this type are of primary importance in determining A/D requirements. Future systems will utilize multiple beam-forming antennas to null out interfering signals and to provide multiple user capability. These systems will use either on board digital adaptive nulling or remote beamforming and nulling with a digital downlink, as in the TDRSS AGIPA system. A phased array with 5 to 20 elements is a likely candidate for this system. If the beam forming is done digitally, then the A/D converters require an extremely large dynamic range (12 or more bits) and a sampling rate commensurate with the signal bandwidth. The reason for large dynamic range is that the individual beam forming elements look at the whole earth at one time.

Although a change to SHF or EHF frequency bands would provide more available bandwidth for spread spectrum, there are good reasons to continue in the present UHF band. The present FLTSATCOM operations use the UHF bands, and approximately 1800 terminals are deployed. It is desirable to minimize the impact on the users. Thus, a simple spread spectrum add-on to the present UHF terminals seems like a reasonable upgrade.

Spread spectrum options such as frequency hopping within a 64 MHz bandwidth appear feasible. This mode is easiest to coordinate on a network basis and permits simple dehopping processing on the satellite if the users are channelized on a coordinated hop basis. Some narrowband hybrid PN might be used also to protect against multiple tone jammers.

The potential jammer threat to such a system as that postulate here drives the component requirements such as A/Ds. This threat can be deduced from the parameters already stated. With a spread spectrum bandwidth of 25 kHz, a single channel realizes a spread spectrum gain of 34.08 dB in dehopping. In addition, the ratio of channel bandwidth to 75 bps data rate makes another 25.23 dB improvement possible. Antenna null depths of 30 dB are feasible with adaptive control and renulling on every hop. Finally, if the user has a 30 dBw EIRP and needs an $E_b/N_o$ of 9.3 dB, the potential threat that the system can meet is jammer EIRP of 110 dBw.

| | | |
|---|---|---|
| Spread spectrum | $\frac{64\ \text{MHz}}{25\ \text{kHz}}$ | 34.08 dB |
| FLTSATCOM processing | | 25.23 dB |
| Antenna null depth | | 30.00 dB |
| User EIRP | | 30.00 dBw |
| Required $E_b/N_o$ | | 9.3 dB |
| Potential Jammer EIRP | | 110.0 dBw |

The dynamic range requirements of the A/D should match the expected performance of the projected system. Since the J/S ratio is 80 dB before dehopping and the range of spread spectrum gains is 14.08 to 34.08 dB, depending upon the number of user accesses (1 to 100 users) the limits of dynamic range required of the A/D are 46 to 66 dB. The dynamic range is directly related to the resolution and loading of an A/D converter. The resolution necessary, in this case, is from 10 to 12 bits.

The sampling rate requirements are determined by the number of accesses and the method of implementing the A/D in the system. Figure 2-5 summarizes the requirements versus capabilities with a 1 Msps rate and with a 5 Msps rate. This graph shows the number of 25 kHz channels that can be accommodated versus the number of antenna elements per A/D converter. Two implementation choices are available: a single A/D converter, timeshared between elements, and multiple A/D converters, up to one per element.

The first of these two options is preferable, because it minimizes the null degradation and beam-steering errors caused by phase and amplitude mismatches between elements. However, the second option could be tolerated with strict tolerances on matching between A/D units. The resulting capabilities are summarized in Table 2-1.

The downlink bandwidth requirements for a remote nulling system are not excessive, even when the digital downlink is used. The present state of the art in downlink bandwidth is probably TDRSS. This system uses an FDM downlink of 650 MHz at Ku-band for telemetry of a 30 element AGIPA remote beam forming link and a single access K-band return link from synchronous orbit. The AGIPA remote link alone requires 224 MHz bandwidth.

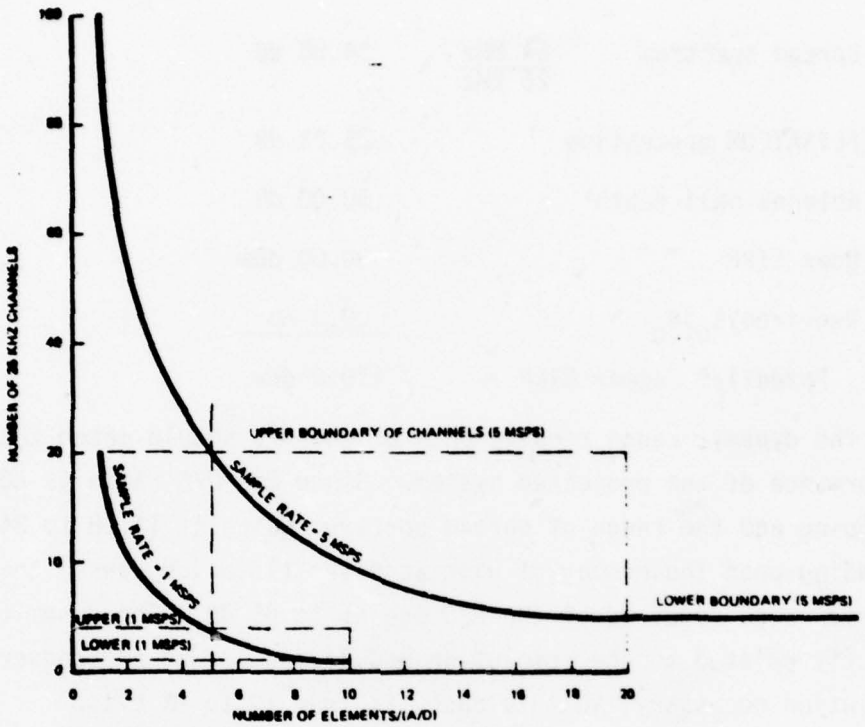



Figure 2-5. Sampling Rate Requirements

Table 2-1. Capability Versus Sampling Rate

| CAPABILITY | SAMPLING RATE (MSPS) | ONE (A/D) PER ELEMENT | ONE (A/D) PER FIVE ELEMENTS | ELEMENT LIMIT FOR ONE (A/D) |
|---|---|---|---|---|
| PRESENT | 1 | 20 CHANNELS | 4 CHANNELS | 10 ELEMENTS AND 1 CHANNEL |
| FUTURE | 5 | 100 CHANNELS | 20 CHANNELS | 20 ELEMENTS AND 5 CHANNELS |

If one single 12-bit A/D converter per satellite is used, with a 5 Msps rate, the downlink bandwidth required is 60 to 120 MHz depending on the modulation technique. If one A/D per element is used, the present units would require 60 to 120 MHz for five elements and 20 users. A future 5 Msps rate would permit 100 users and five elements in a bandwidth of 300 to 600 MHz, again depending on the modulation method.

It is clear that a 12 bit, 5 Msps A/D converter will provide a more economical adaptive multibeam capability. This should make possible achievement of the economically balanced implementation of the combined spread-spectraum/adaptive nulling technique within the parameter limits considered worthwhile and feasible.

### 2.1.6 Wideband Spread Spectrum Receiver

Figure 2-6 is the block diagram of a typical wideband spread spectrum modem receiver that provides jamming protection for compressed video data. The biphase modulated signal on a 7370 MHz carrier is dehopped and converted to a 70 MHz IF frequency at the down converter. The 70 MHz signal is subsequently processed in a 70 MHz IF strip, which provides gain, gain control, and final IF bandlimiting. The signal is again down converted, in the quadrature A/D converter (Figure 2-7), to baseband in-phase and quadrature (I and Q) components. These I and Q signals are each quantized to two bits at a rate of up to twice the cover PN code rate. A gain control voltage (Figure 2-7) is derived just prior to the A/D converter and is fed back to the 70 MHz IF strip to control the loading of the A/D converters.

To gain better insight into the receiver operation, a brief description of the baseband signaling waveform generated by the transmitter follows. Data to be transmitted is convolutionally encoded and pseudorandomly block interleaved. The interleaving scheme provides protection against burst errors. A block interleaver was selected because of its compatibility with the video data format. Frame sync bits are then periodically multiplexed with the interleaved data to allow reconstruction of the video frame sync signal by the receiver. This data stream is then grouped into 2, 3, or 4 bit symbols that are encoded into a 4-, 8-, or 16-ary cycling code corresponding to the transmitter input data rate selected. To provide cover, the encoded data is then combined mod-2 with a PN code. Periodically, the transmitter transmits PN code without data for one hop time over a prescribed pseudorandom dither range during each period. The PN only code transmission is only used by the receiver for acquisition and tracking of the PN code. It is this composite data stream that forms the baseband signaling waveform that biphase modulates the transmitted carrier.

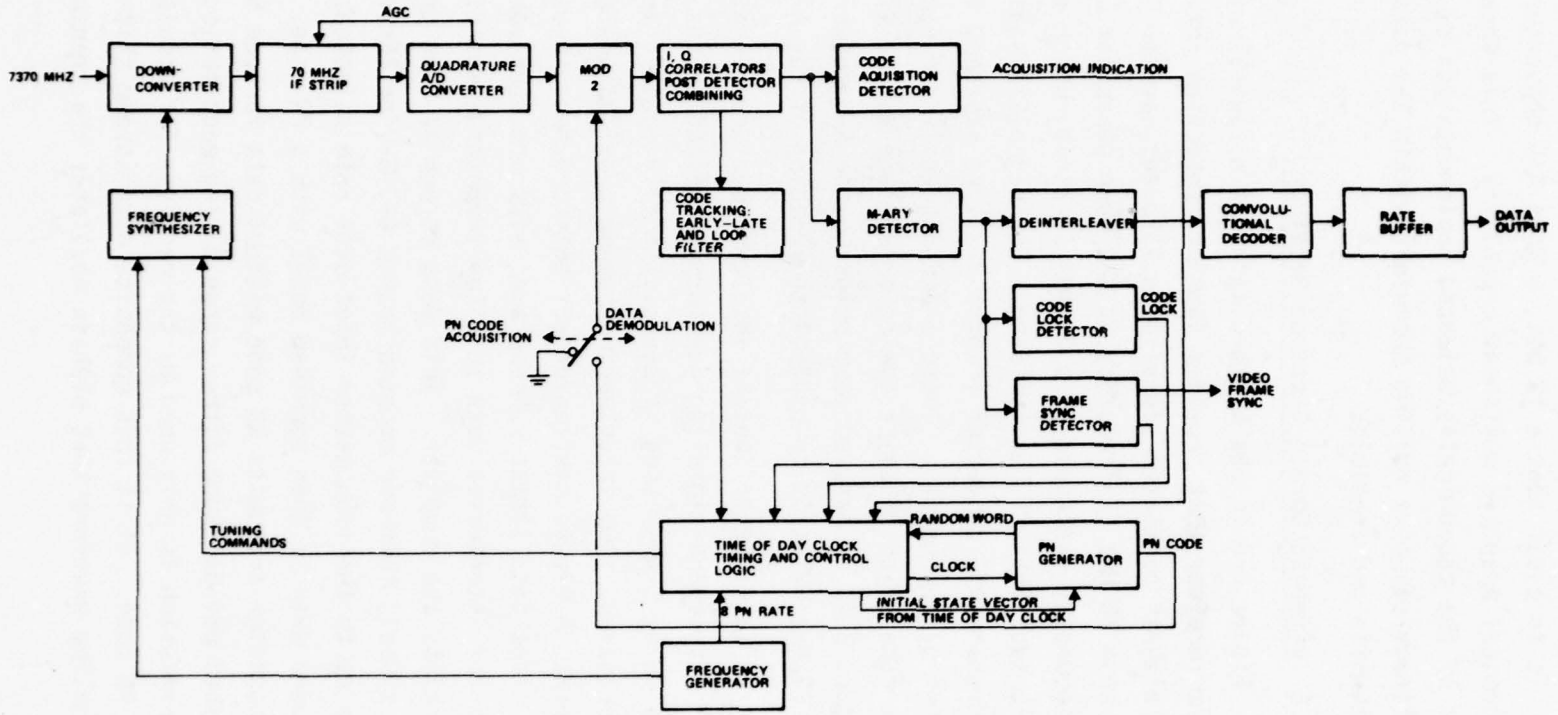



Figure 2-6. Wideband Video Modem Receiver Block Diagram

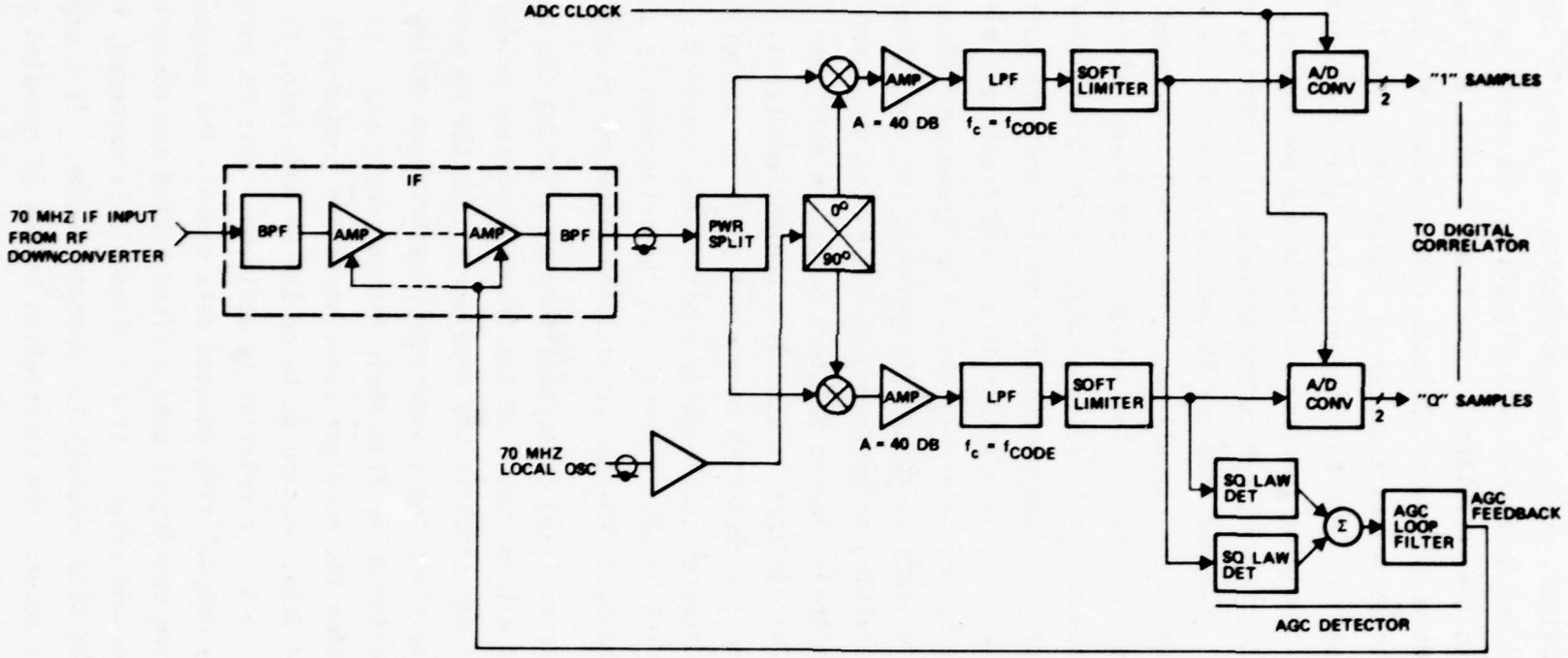



Figure 2-7. IF Strip and Quadrature A/D Converter

At the receiver, during data modulation, PN code is wiped off the two bit quantized I and Q channel data signals by the mod-2 gate (Figure 2-6) and then sent to the correlators. The I and Q correlator banks are used to determine the magnitude of the data code received for each of the M possible code shift values that can be transmitted. The I and Q correlator magnitude outputs are then envelope-detected ($\sqrt{I^2 + Q^2}$) and sent to the post detection combining function (multiple hop per symbol, low data rate cases). The largest of the M code magnitudes is picked by matching the incoming signal, sampled once per PN code chip against the M possible shifts of the data code in the correlators. The symbol is decoded from the magnitude in the M-ary detector. The output of the M-ary detector is the same as the signal input to the cyclic encoder in the transmitter. The signal is then deinterleaved, convolutionally decoded and rate buffered back to the original rates input to the transmitter. The frame sync bits are stripped off the signals before deinterleaving. The frame sync generator from which the end of frame state is decoded to generate the video frame sync pulse output. Code tracking is performed at the PN (no data) hop that is periodically transmitted. The correlators output an early and late magnitude sample of the PN code that is used by a conventional early/late tracking loop to maintain the proper PN code clock phase for the digital processor. The code lock detector continuously monitors the received code magnitude and integrates the values received. If the integrated values fall below threshold the receiver PN code acquisition algorithm is activated.

Receiver acquisition is accomplished by aligning the receiver's time of day clock to within 3 msec of the transmitter time of day clock. Aligning the time of day clock in the receiver aligns the PN code to within the same uncertainty since the transmitter/receiver each derive the PN code state vector periodically from their time of day clock. At the local PN (no data) hop time the receiver correlators are loaded with the local PN code. Received data, sampled at twice the PN code rate, is shifted through the correlators until correlation is achieved. This PN threshold crossing is validated by demodulating encoded data symbols and accumulating code shift correlation magnitudes over a fixed period and comparing the magnitude sum with a threshold value. If the threshold is exceeded, PN code sync is declared and the data demodulation process begins. If a signal dismissal (no validation) occurs, the correlation search is repeated as above.

An alternate implementation of Figure 2-7 would be to move the soft limiters and A/D converters forward in the system to replace the I/Q mixers. The A/D converter will now perform both the conversion to baseband and the signal quantizing. The A/D converter output will be indistinguishable from that which would be obtained in the implementation of Figure 2-7. The savings in equipment would be the mixers and lowpass filters (LPF). The amplifiers would still preceed the soft limiters.

## 2.2 RADAR SYSTEMS

Radar systems are a part of all Navy vessels and aircraft. These systems require a wide variety of A/D converters. Table 2-2 lists some relevant current radar programs and the A/D converters required.

### 2.2.1 Radar System Requirements

#### Synthetic Array Radar

Synthetic array processing provides high resolution groundmapping radar by simulating an effectively large antenna by signal processing rather than by actually using a large antenna. Vehicle motion translates the (relatively small) physical antenna to sequential positions along a line, and at each position a signal is transmitted, received, and stored. These signals can be I-Q sampled before processing to obtain amplitude and phase relationships.

The signal can be processed directly or recorded for nonrealtime processing. In generating a synthetic antenna, the returns from a number of spatial positions must be combined. This is done by weighting the signals for sidelobe-level control. Letting $S_N$ represent the signal received when the physical antenna is at the Nth position of the antenna array, $W_N$ the weight applied to $S_N$, and $\emptyset_N$ on the phase adjustment of $S_N$ required for focusing, the focused pattern is

$$P = \Sigma S_N W_N e^{j\emptyset_N}$$

This focusing can be performed by recirculating delay lines, digital filters, or transforms (FFT or FHT). The requirements are for 6 bit and higher resolution.

Table 2-2. Current A/D Requirements for Radar Application

| RESOLUTION (BITS) | SAMPLE RATE (MSPS) | INPUT LEVEL (VOLTS) | LOGIC LEVELS | PROGRAM | APPLICATION |
|---|---|---|---|---|---|
| 12 | 50 | ±1.0 | ECL | AOSP | SPACE-BASED RADAR |
| 12 | 0.4 | ±1.0 | TTL | TWS | TAIL WARNING RADAR |
| 11 | 1.0 | ±1.25 | TTL | F-16 | RADAR |
| 10 | 10.0 | – | ECL | AFAL | ADVANCED RADAR |
| 10 | 5.0 | ±2.5 | TTL | ARPS | APS-125 RADAR |
| 10 | 1.75 | ±1.25 | TTL | F-16 | RADAR |
| 8 | 50.0 | – | ECL | – | ADVANDED RADAR |
| 8 | 10.0 | ±1.0 | ECL | AWCS | RADAR SYSTEMS |
| 6 | 100.0 | – | ECL | AFAL | ADVANCED RADAR |
| 6 | 25.0 | ±1.25 | ECL | – | ADVANCED RADAR |
| 6 | 12.5 | ±1.024 | ECL | EAR | ELECTRONICALLY AGILE RADAR |
| 6 | 3.5 | – | ECL | F-16 | RADAR |

Radar Processing Array

This form of radar uses a small matrix of driven antenna elements (perhaps 6 x 4) in which the various received and transmitted signals can be phase controlled to vary the antenna pattern or null-out an undesired signal. A block diagram of an adaptive processing array used to null-out interfering signals is given in Figure 2-8. Each of the K array elements has an A/D converter. The K inputs are input to the K element control loops. The Kth control loop multiplies the Kth input and the adder output, then integrates the result. If used, a steering control is added to the integrator output. After amplification the loop output is again multiplied by an array output $X_K$ and input to an adder. The adder weights can also be adaptive to further process the signals. Since the K signals must be preserved in a complex form, the block diagram shown in reality has I and Q channels.

Following the array summed output, MTI processing is performed digitally. Since the A/D converter output is used for the feedback loop, a poor design could result in instability. Therefore, the A/D converters used must be monotonic, provide fine resolution, have low sample-to-sample memory, and must sample all array elements simultaneously.

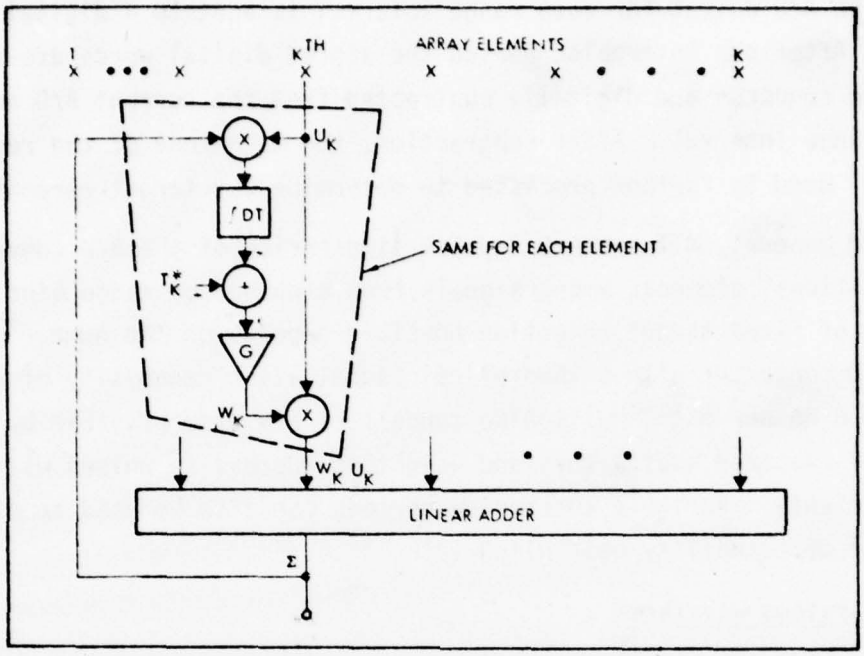



Figure 2-8. Implementation of Element Control Loop for an Adaptive Array Functional Block Diagram

MTI Radar

The APS-125 radar is an MTI system that uses digital signal processing for detecting moving targets in a background of clutter. Clutter is distinguished from targets by virtue of the difference in their spectra. The degree of clutter rejection achievable is a function of the number of A/D bits. Implied resolution must be adequate to provide higher cancellation than the limitations imposed by other radar system parameters, particularly antenna scanning modulation. The APS-125 uses a 10 bit A/D converter to achieve a cancellation ratio in excess of 50 dB. Four time-synchronized A/D converters perform sum and difference IQ sampling to prevent blind velocities. The system timing relationship between the transmitter pulse, and sampling instant of the four A/D converters is synchronized by a preset signal from the processor which resets the A/D converter and starts the sampling process. To prevent a loss in detectability the A/D converters sample at least two times in a pulsewidth interval. This requires a sampling rate of 5 Msps.

The A/D output for each range interval is sent to a digital storage unit. After one interpulse period the stored digital words are read out in time sequence and digitally subtracted from the current A/D output for each range interval. After subtraction, the magnitude of the resulting digital word is further processed to determine key target parameters.

In general, MTI systems involve timesharing of the A/D converter and computational elements among signals from a number of range bins. The degree of fixed target rejection possible depends on the number of bits in the A/D converter with a theoretical cancellation capability of approximately 6 dB per bit. Multipulse cancellers are also possible by using several cascaded subtractors and weighting successive pulses with binomial coefficients. Variable interpulse periods can also be used to minimize the loss of detectability near blind velocities.

Radar Systems Waveforms

The requirements imposed on radar system waveforms are determined by radar function, i.e., search, track, wake discrimination, search in clutter, chaff cloud mapping, etc. These radar waveforms, in turn, may be conveniently grouped into classes such as: single linear chirps, uniformly spaced bursts, non-uniformly spaced bursts and coherent pulse pairs.

The waveform parameters of particular importance with respect to radar signal processing are: sub-pulse duration, sub-pulse bandwidth and burst durations, signal to noise ratio and sidelobe/spurious levels. The above parameters directly or indirectly influence the two most significant A/D Converter parameters, resolution and speed.

### 2.2.2 Potential High Speed A/D Applications

The application of analog-to-digital converters basically involve those radar systems which measure shape, change of shape and size.

Measurement of the return signal amplitude as a function of position, frequency, and time is not as commonly used in radar as similar measurements made with phase. The measurement of phase variations is more germane to the behavior of the target as if it were a point source, while the measurement of amplitude is more appropriate for investigating the size and shape of the target.

The relationship between the signal-to-noise ratio, the probability of detection and the probability of false alarm is fundamental in any radar system. Many pulses are usually returned from any particular target on each radar scan and integration of radar pulses can be used to improve detection. All practical integration techniques employ some sort of storage device or signal processing. Integration can be performed by electronic devices, in which detection is done automatically on the basis of an adaptive threshold crossing.

Predetection integration requires that the phase of the return signal be preserved if full benefit is to be obtained from the summing process.

The analog-to-digital converter is a potential candidate for this predetection integration. In this application, a signal-to-noise ratio of 18 db is adequate to assure a probability of detection of 0.9999 and a probability of false alarm of better than $10^{-12}$. A 6-bit A/D converter will provide adequate resolution for a dynamic range (power) of 18 dB.

The accuracy with which radar range and doppler velocity can be measured depends upon the ratio of the signal energy to noise power per Hertz, just as it does for the probability of detection. Therefore, reliable detection and accurate measurement go hand in hand.

A high speed analog-to-digital converter can be used to process the doppler video signal to extract moving target echoes using digital subtraction rather than an analog canceller. The above requirement implies a continuous analog conversion process not driven by the radar prf. This technique would eliminate blind speed limitations and range ambiguities. In addition, it may be possible to compensate for clutter from a moving platform, i.e., high speed aircraft or a moving ship.

There are several Navy Radars that require high speed A/D converters of from 5 to 1000 Msps.

Six of these Radars are identified below.

1. There is an exploratory development in radar at the Naval Ocean System Center which processes the digitized video for signal recognition. It employs a pulse length of 0.1 microseconds and employs many sample/pulse. The highest sampling rate that has been considered is 100 Msps.

2. Naval Research Laboratories is building a synthetic aperative radar for anti-submarine warfare. Presently A/D converter requirements are 100 to 200 Msps at 4 to 6 bits.

3. Naval Research Laboratories is building a high range resolution monopulse tracking radar (not synthetic aperture) that requires an A/D with 100 to 800 Msps and 6 to 8 bits of quantization.

4. Naval Research Laboratories is also working on an adaptive array program which involves from 20 to 200 channels with a sampling rate of 5 MHz at 10 to 12 bits quantization. The system requires A/Ds matched in bandwith, simultaneity, and throughput delay. For a given system of adaptive array processors the A/D converters must be matched and stay in match over temperature and time.

5. The Naval Weapons Center at China Lake, California, has been working on a high resolution synthetic aperture radar (SAR). NRL is said to have a parallel interest in the concept. They wish to provide 2 foot range resolution. The A/D requirements are in the range of 50 to 250 MHz sampling rate with a quantization of about 8 bits.

6. TRW of Redondo Beach, California, is working on a range profile identification system radar project employing very fine resolution. High speed digital computations are performed and the resulting profile is compared with a library of profiles for identification purposes. Every 20 nsec there is a measurement which roughly corresponds to 20 feet.

Advanced Radar Systems

The current and projected advances in high speed microelectronics suggests that the traditional analog/digital partitioning of airborne radars should be reexamined. Currently 400 Msps A/D converters, which are capable of direct IF sampling, are in the developmental stage. Together with high speed digital processors this allows processing directly at the outputs of phased array elements. Digital filtering will make adjustable filter bandwidths available for different radar modes, and provide improved jammer rejection. For spread spectrum radars the digital processing can perform despreading of the radar returns.

Advanced concepts are most suitable for MTI and attack radars. Such a system will consist of a solid state phased array of about 2000 elements with digital signal processing occuring directly at the phased array elements. This system will require extensive use of advanced micro-electronic elements in both the RF and digital circuitry.

Currently beam processing is performed by analog circuitry and is generally restricted to adaptive pattern processing. Digital beam processing will provide greatly increased angular resolution, multiple target track with scan capability and multiple beam and spread spectrum techniques for convert operation.

The advanced radar system block diagram is shown in Figure 2-9. This circuitry is duplicated for each of the antenna elements. The receive section consists of a low noise amplifier (LNA) phase splitter, filters, and 4 bit A/D converters. The LNA can be implemented with a GaAs integrated circuits. It is projected that this circuit could achieve a 3 dB noise figure in an 8 to 12 GHz band. The A/D converter is a 4 to 5 bit GaAs full parallel organization that would require no sample and hold. The sample rate will be 250 to 500 Msps.

The transmit section consists of a digital phase shifter, mixer and high power amplifier. The digital phase shifter is a programmable divider operating at the reference frequency (10 GHz). The divide ratio is programmable from 1 to 16 by a 4 bit command. This circuit would be a GaAs IC utilizing TEDs to achieve the required high frequency performance. The high power amplifier would also be a GaAs circuit. In this case GaAs FETs would be used. Currently high power GaAs FETs are available and it is feasible to integrate a complete amplifier.

It is desirable to integrate the filtering and mixing operations together with the amplifiers. This appears to be possible with GaAs integrated circuits since the process can include FETs, TEDs, resistors, and capacitors. With 2000 elements it is imperative that the maximum degree of integration be achieved to maintain a low cost and resonable size and power.

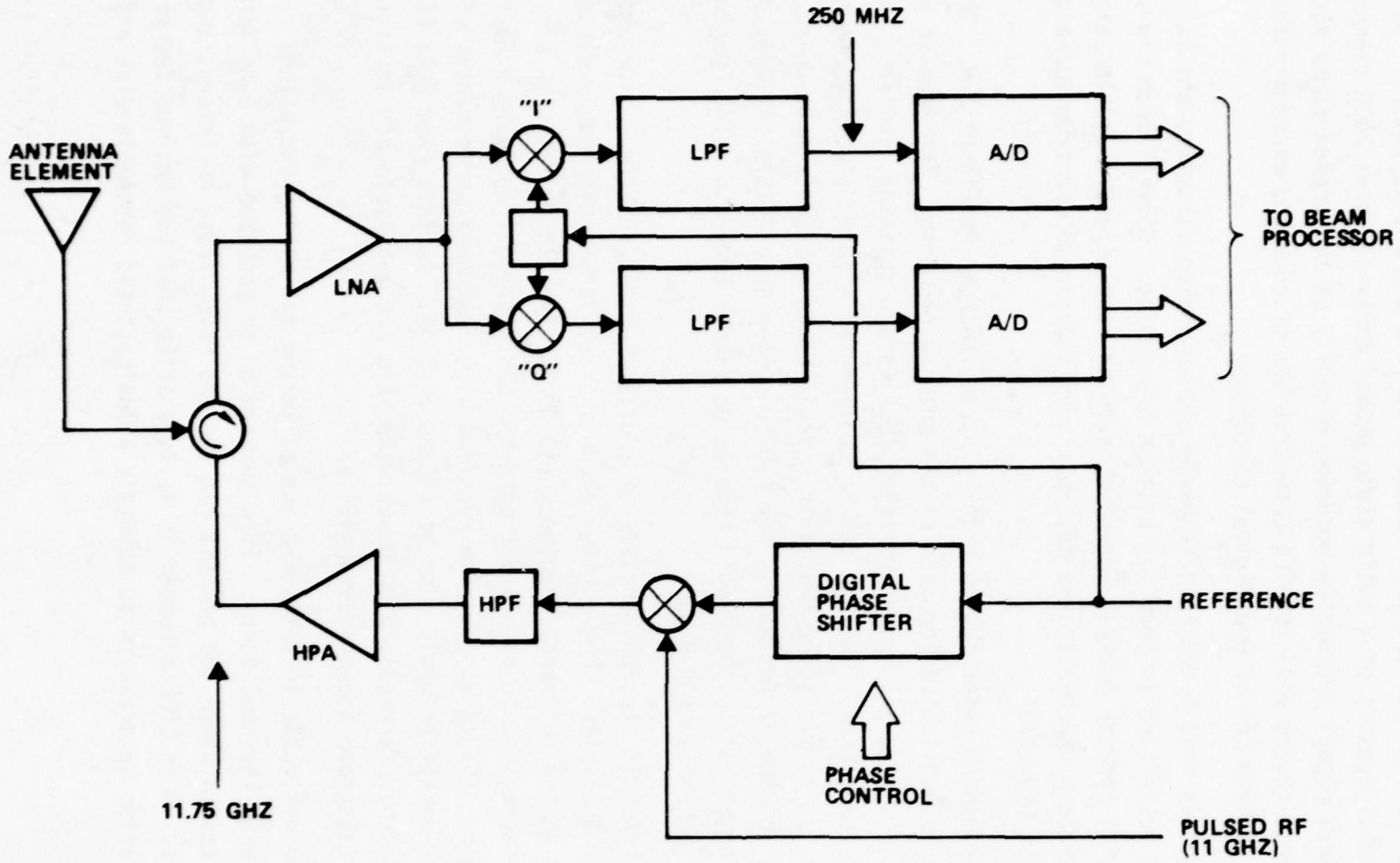



Figure 2-9. Advanced Radar System

Beam processing requires high speed operation because it must be performed on a range bin by range bin basis. The basic arithmetic operation is a complex multiply and add for each of the phased array elements. The complex product can be single precision (4 to 5 bits) but the addition is a summing of all weighted array elements outputs and will result in a 16 to 20 bit aperture output. The best approach is to take advantage of the natural parallelism and distribute the computation over the array elements. The limiting case is a complex multiplier for each array element with an adder network to perform the summations. For this case a system with a 100 nsec range bin period and five summations per range bin period would allow 20 nsec for single complex multiply and add function. Because GaAs multipliers are projected to have multiply rates of 10 nsec this appears to be a practical approach.

## 2.3 OPTICAL SYSTEMS

The advent of high resolution imaging sensors (with correspondingly high data rates) requires precision high speed A/D converters. Such converters operate at baseband and must have low sample-to-sample memories and good differential linearity to provide high fidelity digital picture quality. In applications such as earth observation satellites with multispectral sensors, it is conceivable that a single A/D converter could be multiplexed between spectral band samples. With a pushbutton scanner (line scanning array), multiple A/D converters may be required, one for each element of the array.

### 2.3.1 Optical Sensor Requirements

The techniques used for imaging products can use a variety of technologies. Imaging detectors are either linear image devices (LID) or area imaging devices (AID). One common form of LID is a long single plane device using an array of depletion regions or potential wells that are formed by a MOS-type capacitor to sense and store photo generated charge, with a transferring mechanism to transfer the charge from the capacitor through a register to the detector preamplifier. The easiest way of achieving these functions is to transfer the charge packets serially through the same potential wells that perform the sense and store function. This method, however, introduces image smearing unless either the

transfer is carried out at a speed considerably in excess of the light sensing or integration time or the transfer operation is performed in the dark. When the output data rate is different from the transfer rate, it is necessary to provide an additional buffer store. When this method is used for a rectangular area photoelement array it is called frame transfer. A significant improvement to this technique involves the use of a parallel transfer shift register for the transfer and shifting. Due to the inherent design of the transfer register analog data storage can be achieved.

The AID is simply a two dimensional LID. The techniques used to produce this device are precisely the same as for the LID. Various techniques are used to obtain frame transfer, line transfer and interface transfer.

The frame transfer organization is functionally the simplest. The line transfer structure employs a scan generator, and the interline transfer technique requires separate photoelement sites and shift registers. The interline technique is an improvement over the other techniques because of separate imaging and storage sections which will eliminate image smearing and image streaking.

There are two basic categories of devices based on the way in which the analog samples are handled. In the charge transfer devices (CTD) each sample of charge is transferred from stage to stage across a chip under the control of a sequence of clock pulses. There are two types of these multiple transfer devices, bucket brigade devices (BBD) and charge coupled devices (CCD). The differences between them are primarily in the details of the device structure. From the functional point of view BBDs offer a way to make a practical tapped analog delay line for such applications as correlators and externally programmable transversal filters. The CCD technology is capable of higher sampling rates and higher density devices.

The second major category is the single transfer devices (STD). These devices are similar to an integrated set of multiplexed sample-and-holds. Each successive sample is stored in a separate discrete memory cell, where it stays until it is read out. These devices have applications on video delays, data buffers, and time base correctors.

### 2.3.2 A/D Converter Applications

In optical sensor systems the major A/D converter tradeoff involves the level of multiplexing to be employed. Line arrays generally consist of many individual segments that are simultaneously read out (Figure 2-10). This is necessary to achieve high scan rates. The tradeoff between analog and digital multiplexing is highly dependent on A/D converter capabilities. The main limitation on the level of multiplexing is the speed of the A/D converter. The more analog multiplexing employed, the higher the conversion rate of the A/D. Generally analog multiplexing is more difficult in terms of size, weight, power, and cost than digital multiplexing for equivalent bandwidth and bit rate. As the bandwidth and equivalent bit rate increases, analog multiplexing becomes disproportionally more difficult than equivalent digital multiplexing. This trend must be compared with the optimum (in terms of size, weight, power, and cost) A/D converter speed. Neither a large number of slow A/D converters nor a few extremely high-speed A/D converters is an optimum choice.

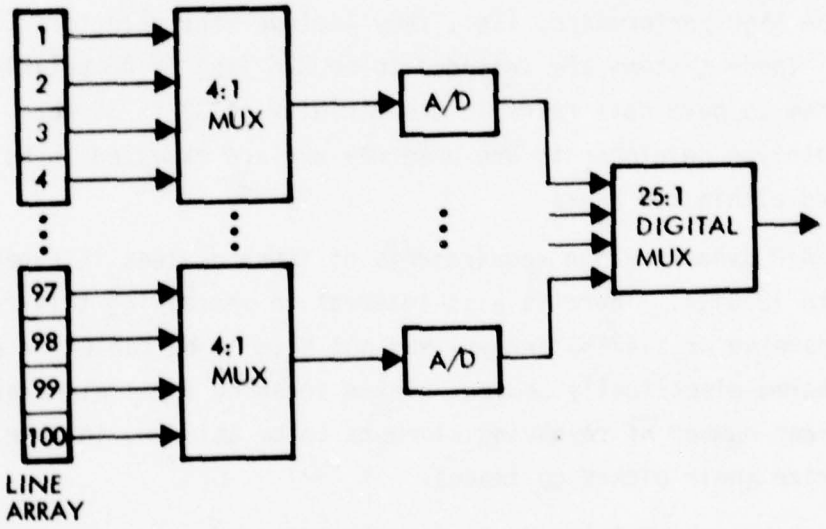



Figure 2-10. Line Array With 4:1 Analog Multiplexing

Current systems require total sample rates of up to 50 Msps at 8 to 10 bits of resolution. The development of low power, low cost, high speed single chip A/D converters is essential to developing low cost systems. It is obvious that the effective use of these A/D converters will require the development of high-speed analog multiplexers with low crosstalk and excellent linearity. An indication of the interest in high speed A/D converters is shown by the fact that NRL is evaluating a 400 Msps 5 bit unit for a classified optical processing program.

### 2.3.3 FLIR Systems

There are at least three types of FLIR (forward looking infrared) applications of high-speed A/Ds within the Navy. They are 1) Second generation imagers employed for ocean surveillance, 2) Class B FLIRs, which are shipborne search sets (classes A, B, and C are defined below), and 3) FLIRs which are part of a classified missile system called FIRE and FORGET.

The second generation systems employed for ocean surveillance employ advanced focal plane arrays. Most of these focal plane arrays are considered to be high-performance, i.e., they include many detectors (10,000 to 20,000). These systems are intended to be 875 line TV compatible. This causes them to have data rates in the vicinity of 33 to 35 Mbps. Brassboard prototype developments are underway and are expected to be completed and tested within two years.

The A/D dynamic range requirements of these devices is expected to be from 10 to 12 bits. There is also interest in increasing this capability for nonscanning or STARING arrays) may not have to be cooled or at least may be thermo-electrically cooled. These advanced focal plane arrays have a sufficient number of resolving elements to be able to, in some sense, characterize their picked up images.

Search sets have fewer resolving elements and, as a consequence, the data rate is less. These search sets are employed for detection and not for imaging. There are numerous Class B FLIRs destinated to be incorporated in the Navy Inventory. One of these is the Far Infrared Camera which has a conversion rate of 20 Msps. Two routes to obtain this conversion rate are being considered:

a. Multiplex 2 A/D converters, each at 10 Mbps sample rate.

b. Use 6 separate detection channels with a multiplex for each. This provides a 3 Mbps sample rate for each channel with a 10 bit resolution.

In the past it has been necessary to break the data flow into parallel channels because of A/D limitations as evidenced in b above. The advent of high speed A/D converters for this application will probably influence the decision to proceed with option a above.

One shipboard sensor system, a design-to-price IR search set, is a multi-channel multiplexer using commerically available equipment including the A/D converters. This system requires a multi-megasample per second conversion rate, 12 bit resolution and 360 degree surveillance. In general, this design will break the data flows into parallel channels because of A/D limitations. The typical numbers quoted for the system are:

- 50 second dwell (pulse length) time. Future requirements will consider 10 second and eventually 1 second dwell times
- Sampling at 2-1/2 times the dwell time with 12 bit resolution
- Channel capacity will be from 100 to 500 parallel channels.

This design is constrained by price and inexpensive successive approximation A/D converters are being investigated. This requirement is now using 10 mega words per second at 8-bit and 5 mega word per second using 36 channels multiplexed. From scan speed considerations, the desire is to go to 10 samples per unit or higher rather than the current 2 seconds per sample.

There is also under development a classified missile called FIRE and FORGET in which the Navy has some interest. This device employs a steering focal plane array. In its present form it employs a FLIR which is 525 to 825 line TV compatible. Eventually, it is expected to be employed with much more advanced higher line/frame TV Systems.

### 2.3.4 Other Optical Systems

The Naval Ocean System Center has ordered a solid state camera of 760 tels (pixels) on a line and 488 line resolution. (T.I. may have a single

chip of comparable resolution.) There are some classified requirements in the areas of:

a. Airborne applications (involving arrays of scanners) optical and IR

b. RPVs which call for very high data rates of 50 to 100 MHz (possibly employing line arrays).

### 2.3.5 Postulated Future System Requirements

Application of image sensors extends over a wide variety of fields and significant new applications can be expected to surface in the next few years. Known applications include accurate, noncontact measurements, facsimile sensing, velocity measurement, surface flow detection, shape recognition, security surveillance, accurate area measurement, position meters, and line of sight detectors. These applications are expanding extremely rapidly with the advent of new device technology. Future systems applications will require up to 1 Gsps conversion rate with a potential 12-bit resolution requirement.

## 2.4 ELINT/EW SYSTEMS

Future Navy ELINT and EW systems will be required to deal with various classes of exotic signals. In general these signals can be grouped into four classes.

1. Spread Spectrum
2. Frequency Agile
3. Narrow Pulse
4. Broadband Noise Jammers

Each of these classes must be characterized in terms of bandwidth, pulse-width, and pulse repetition intervals. In addition ELINT systems will be required to determine instantaneous phase, frequency and amplitude. This information is only available in the receiver predetection IF signal. Processing the IF signal directly often means higher bandwidths must be accommodated. Since it is necessary to use digital processing for signal analysis a very high speed A/D converter and digital processor or buffer memory are required.

### 2.4.1 Signal Characteristics

The characteristics of the four classes of exotic signals impose overlapping constraints of the receiver and processor. Therefore, it is necessary to examine each class to establish the total system requirements.

#### Spread Spectrum

Spread spectrum radar signals have their bandwidth spread by some intra-pulse modulation technique. This is primarily a jamming protection feature that is becoming more widely used in both radar and communications. The most common types of modulation are FM and PM. A typical PM system uses biphase coding where the RF phase is shifted in discrete 180 degree steps by a pseudorandom binary sequence. Future systems may use polyphase coding where the RF phase is shifted randomly in 90 or 45 degree steps. The FM systems are mainly chirp radars where the RF is swept within the pulse interval. The sweep may be either linear or nonlinear, however, linear is the most common.

To characterize a spread spectrum emitter it is necessary to determine the type of modulation and coding being used. The main parameters of interest for a PM system are pulsewidth, subpulse width, type of code, length of code, and phase modulation format. For an FM signal the parameters are FM bandwidth and waveform (linear or nonlinear).

Measurement of these parameters requires a wide RF bandwidth, high frequency measurement accuracy, wide video bandwidth and high speed digital processing. The RF bandwidth must be wide enough to accommodate the expected emitters. It is estimated that future systems may require bandwidths of up to 1 GHz. To accurately determine the modulation characteristics requires high frequency measurement accuracy. This is true of both biphase and chirp signals since they are either very stable or coherent. Accurate frequency measurement will also be required for future systems using nonlinear FM or coherent frequency hopping.

Frequency Agile

Frequency agile emitters have their carrier frequency hopped or continuously tuned between pulses or groups of pulses. To characterize a frequency agile emitter it is necessary to measure RF range, sweep rate or hop rate and sweep or hop pattern. The best approach appears to be an instantaneous frequency measurement (IFM) system. The instantaneous bandwidth must be as wide as the maximum signal bandwidth. Here again the bandwidth required for future systems could be up to 1 GHz. A major processing problem associated with frequency agile emitters in a dense environment is the necessity to sort large numbers of pulses in order to identify those associated with a single emitter. This requires complex signal sorting algorithms and large memories. The sort must be accomplished before the emitter characteristics can be determined.

Narrow Pulse

Narrow pulse signals (pulsewidth <100 nsec are primarily used in high resolution radars. Radars with pulsewidth between 50 and 100 nsec are common and the number in operation is rapidly increasing. Making accurate measurements of pulsewidth and PRI would require an A/D sample rate of 100 megasamples/second. However, measurement of the detailed waveform envelope (rise time, pulsewidth, etc.) of future narrow pulse signals will require a

bandwidth of at least 500 MHz. Sampling the predetection IF signal will then require a sample rate of 1.25 gigasamples/second. This would allow pulses as narrow as 4 nsec to be characterized.

Broad Band Noise

Characterization of bradband noise jammers is an increasingly important part of an ELINT operation. Noise jamming is typically produced by modulating an RF carrier with a broadband noise source. The modulation may be either frequency or amplitude. The important parameters are RF bandwidth, modulation signal, and RF sweep range. To accurately process broadband jammers a bandwidth of up to 1 GHz will be required. Precise measurements of instantaneous frequency and amplitude are necessary to full characterize the modulating signal type and rate. Long sample times will be required to deal with low frequency modulation signals. This suggests large memories or complex processors.

### 2.4.2 Wideband Collection Systems

The characterization of the signals discussed in the previous section requires that the receiver IF signal be digitized and processed. An ELINT system will typically record the detected IF with very little or no real time processing being performed. The recorded signals will later be processed by large ground based computers. In a tactical situation real time processing is required to direct counter measures. Since tactical aircraft are severely limited in both space and power the receiver and processor must be both compact and low power. With standoff jammers the size and power constraints are less severe.

A simplified wideband collection system is shown in Figure 2-11. The predetection IF bandwidth is 500 MHz to 1 GHz. This requires the A/D converter to sample at 1.25 to 2.5 gigasamples/second. Since the dynamic range of the IF signals is typically 30 to 45 db, 6 to 8 bit resolution is required. The total output bit rate of 20 gigabits/second greatly exceeds even projected memory capabilities. It is necessary to use a data expander to slow down the data rate to an acceptable speed. The required memory size is somewhat dependent upon the type of signal being processed. If it is assumed that a minimum of 100 msec is adequate for all signal types the memory size is then 2 gigabits.

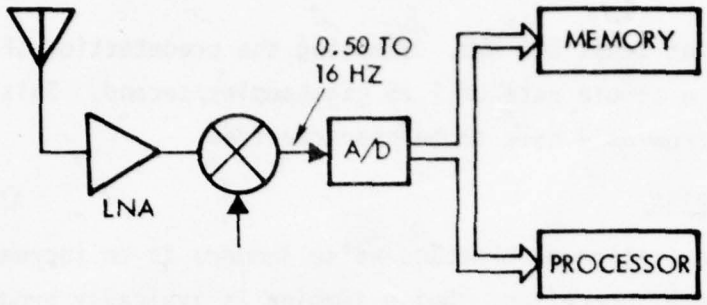



Figure 2-11. Simplified Wideband Collection System

A second approach (Figure 2-12) uses IQ sampling to reduce the A/D converter sample rate. In this case the sample rate is 750 megasamples/second to 1.25 gigasamples/second. This approach does not reduce either the memory size or the processor data rates. The data from the A/Ds must first be multiplexed into a single stream before it can be processed. An additional consideration is that the IQ A/D converters must be matched and track in sample time, gain and phase.

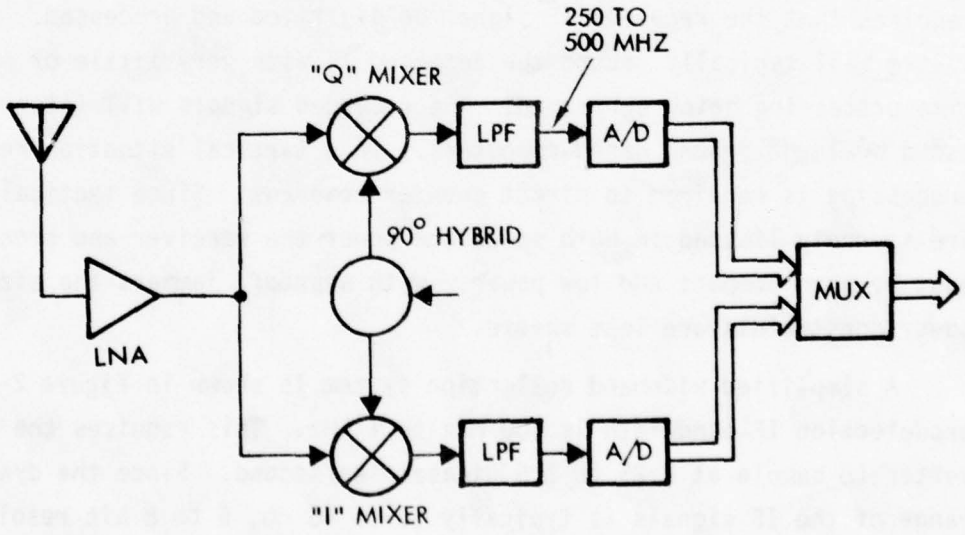



Figure 2-12. Wideband Collection System Using IQ Sampling

A practical system must have an adequate RF bandwidth (500 MHZ to 1 GHz), wide tuning range (2 to 20 GHz) and real time processing or data storage. One such system is shown in Figure 2-13 where two predetection IF signals with a 500 MHz bandwidth provide real time coverage of a 1 GHz bandwidth. The IF signals are digitized at a 1.25 GHz rate with 8 bit resolu-

tion. The digitized data is then transformed by a 1024 point FFT. The output of the FFT is further processed by an associative processor to identify and classify received signals. The 500 MHz bandwidth and 1.2 MHz resolution provided by the A/D and FFT is adequate for present environments and will provide for coverage of 70 to 90 percent of projected future systems.

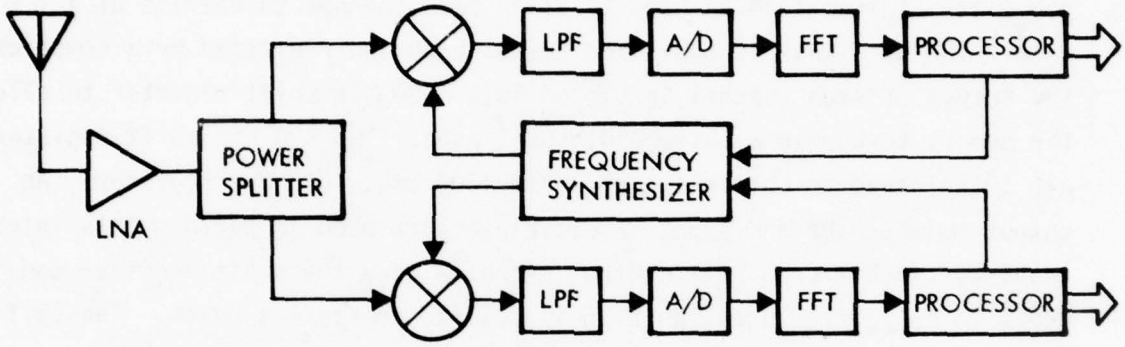



Figure 2-13. Wideband Collection System With Processor

The processor classifies and identifies emitters, records the location, locates new emitters, and controls receiver tuning. In a tactical situation it can identify threats and control counter measures. A tactical aircraft would only need one 500 MHz IF to handle most environments, if the processor were programmed to process only the local expected emitters.

This approach eliminates the need for large memories since only data on new emitters and the occurrence and location of known emitters is recorded. However, advances in memory technology specifically electron beam addressable memory (EBAM) and magnetic bubble memories will make large memories practical and cost effective for many ELINT systems.

### 2.4.3 RF Memory

Future EW systems can benefit from the use of a digital RF pulse memory for radar jamming systems. A digital pulse memory would require less hardware than existing RF loop memory elements in repeater jammers and would offer several other important advantages. The storage time available from a digital memory is near infinite and widely variable. This capability would allow the jammer to handle PRI agile radars and to utilize smart jamming techniques based on a variable, return pulse delay. The high

fidelity of the digital memory would allow the jammer to be equally effective against CW, pulsed, chirped or phase coded emitters. The bandwidth of a high speed digital pulse memory could be made sufficient to deal with frequency agile radar systems.

A block diagram of a 1000 MHz BW RF pulse memory is shown in Figure 2-14. IQ sampling is used to allow each channel to operate at a 1 GHz rate. The RF signal is converted to baseband and digitized by a comparator. The output of each channel is stored in a 1000 bit shift register to allow the memory to handle a pulse width of 1 μsec. Two 500 bit shift registers are interleaved to obtain the required 1000 bit, 1000 MHz register. An output multiplexer and input demultiplexer are used to perform this interleaving. A shift register control signal allows the shift register contents to be recirculated, when it is desired to store a pulse. The shift register output drives a D/A converter to convert the stored digital pulse back to a baseband analog signal. A mixer reconverts this to RF. Future RF pulse memory systems can use GaAs technology to provide an even wider bandwidth at a lower power consumption without the need for IQ sampling.

### 2.4.4 Tactical Low Band ESM System

The desire to improve and extend the capability of existing ESM systems has fostered an interest in using communications and telemetry signals to assist in identifying potential threats. NADC at Warminister, Pennsylvania, has one such system in the early stages of development. The system uses IF predetection processing on a wide bandwidth to handle spread spectrum and frequency agile communications.

The NADC system covers the frequency range of 50 to 850 MHz in four 200 MHz bands. The incoming signal is down converted to a 200 MHz IF, and then digitized by an 800 Msec/sec 6 bit A/D converter. The A/D output is stored in a high speed buffer memory. Subsequent processing includes an FFT unit, a parallel array processor and a control microprocessor. The system also includes a direction finding array consisting of three narrowband receivers and A/D converters. The actual signal location will be performed by the FFT and the control microprocessor. A block diagram of this system is shown in Figure 2-15.

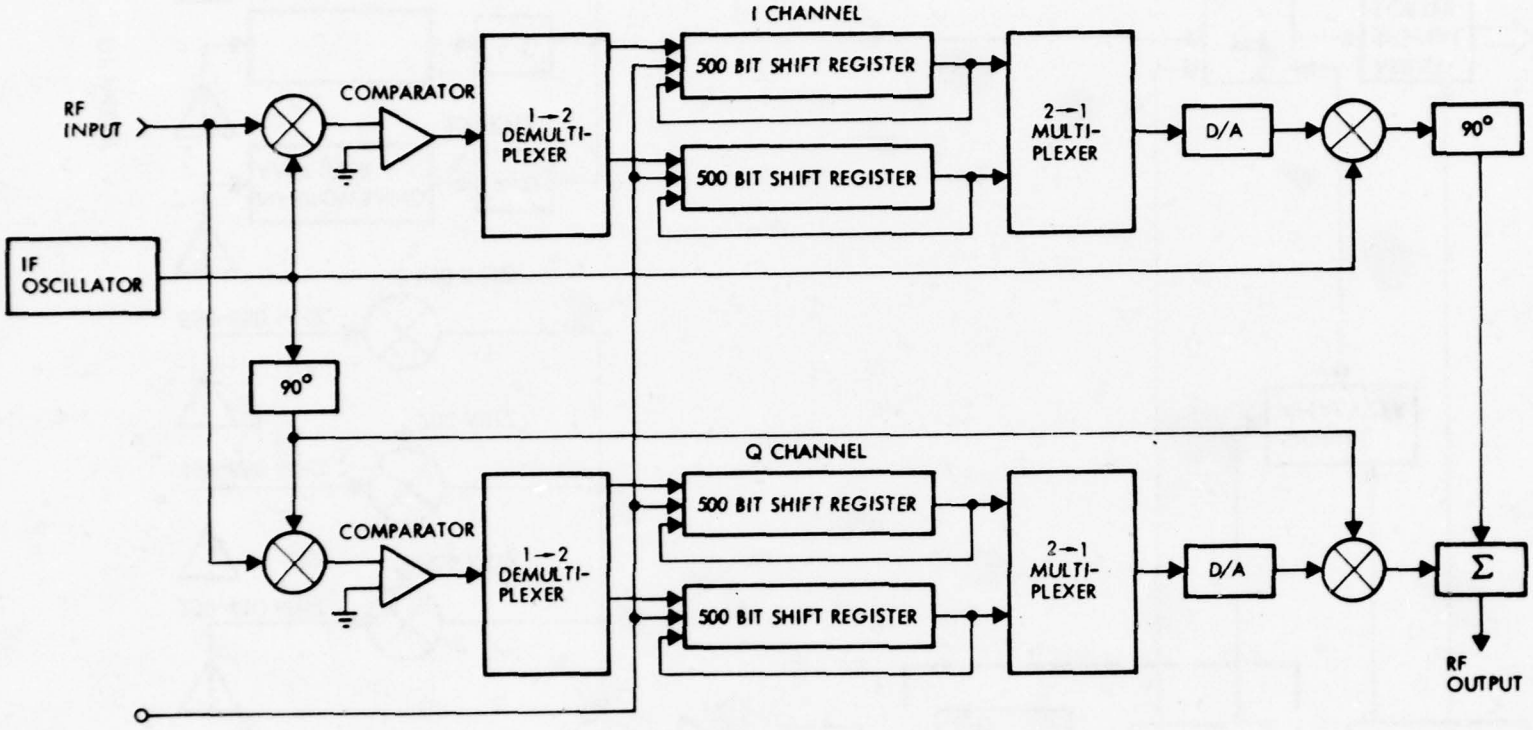



Figure 2-14. RF Memory System Using Existing ECL

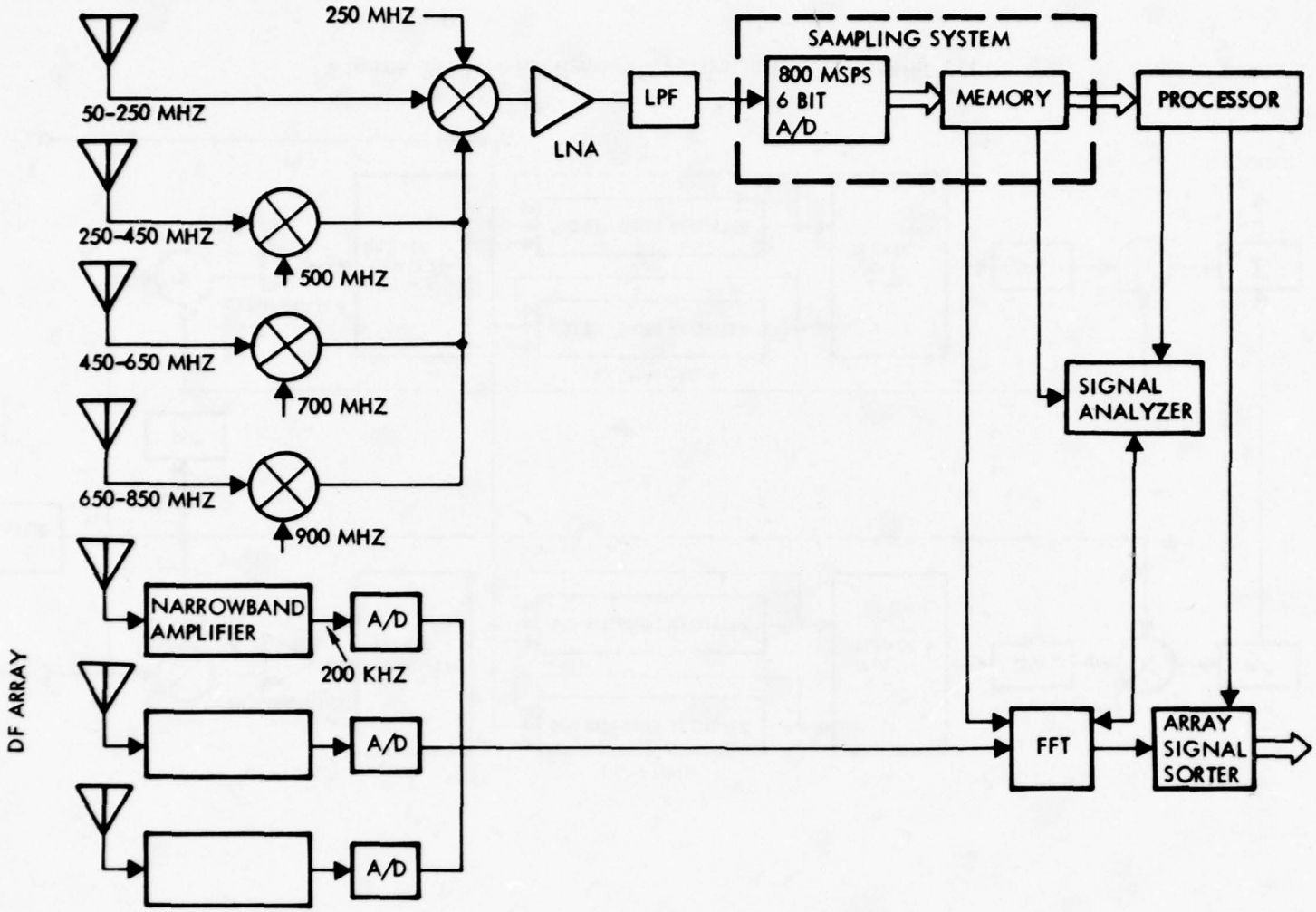



Figure 2-15. Tactical Low Band ESM System

The current sampling system was developed by Aeroflex Laboratories Inc. The system includes an 800 Msps 6 bit A/D, a data expander and a memory for storing up to 16K 6 bit samples. The A/D utilizes 8 interleaved 100 Msps 6 bit A/Ds with the outputs multiplexed to provide a 6 bit parallel gray code. To achieve the 800 Msps sample rate the 8 A/Ds are sequentially strobed at 1.25 nsec intervals. A block diagram of the A/D is shown in Figure 2-16. The A/D is approximately 15 x 9 x 16 inch and the total system (A/D and memory) requires 1 kW of power. This is a very complex system with a high parts count, high power, and will be difficult to maintain.

The interleaved A/D approach has two major drawbacks. First the individual A/D must be matched in both gain and phase. Any small mismatch reduces the performance drastically. Six bit performance requires that the interleaved A/D's must be matched to better than 0.1 dB in gain and 1 degree in phase. Second the instant of sampling must be precisely fixed and uniform. A nonuniform sampling interval is equivalent to aperture jitter and will also reduce performance. If the relative timing between the 8 A/Ds was set to 10 percent accuracy ($\pm$125 ps) the SNR performance would be limited to 26 dB or about 4 bits. To achieve good 6 bit performance the timing and any associated jitter must not exceed 12.5 ps rms.

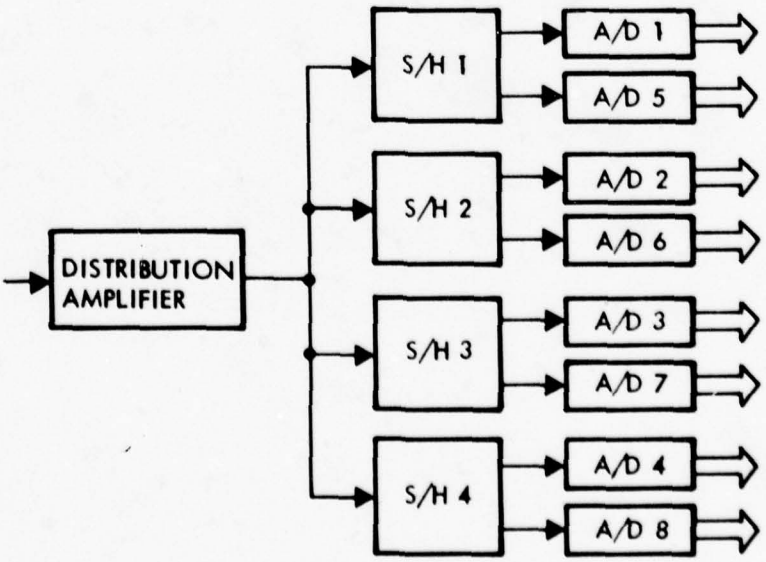



Figure 2-16. 800 Msps A/D Converter

The initial adjustment of gain, phase and timing is difficult, however the major problem is maintaining these settings over any reasonable temperature range. NADC is initiating a hybridization program that will reduce the A/D size and alignment problem but should not be expected to greatly reduce the power consumption since the same components will be used.

This system could greatly enhance the capability of existing and future ESM systems. In the environment projected for the 1980's and 1990's this capability may be absolutely essential to accurately evaluate threats and direct counter measures. For this to be a viable tactical system will require that the A/D converter be reduced in size, complexity and power. The memory size and power must also be reduced or alternately a real time processing capability be provided.

### 2.4.5 Conclusions

There are currently a significant number of A/D requirements in the 100 Msps 6 bit range for various EW and ELINT systems. This requirement will persist for most near term developments. Future systems will require sample rates in the 1 to 2 Gsps region at 6 to 8 bits. High speed memories and processing elements will also be required to support these data rates.

## 2.5 SONAR SYSTEMS

Modern sonar systems have adopted many of the same techniques used in radar systems. These include beam forming, complex signal processing and IF sampling. One new sonar system (SADS), being worked on at the Naval Avionics Center, uses 240 beams and requires low cost low power 2 Msps 12 bit A/D converters. This system is being developed by Naval Avionics Center. Sonar system A/D requirements are characterized by medium speed (2 to 5 Msps) and wide dynamic range (10 to 12 bits).

### 2.5.1 Sonar System Requirements

Sonar signals, whether the echoes of active sonars or the target sounds of passive sonars, must always be observed amid a background of noise or reverberation. The sonar system must detect the presence of the signal in this background.

In the design of receivers and displays, the objective is to achieve the minimum detection threshold consistent with system requirements, among which are a detection probability and false alarm probability compatible with the practical use of the sonar. For minimum detection threshold it is desirable to use the longest signal duration permitted by system consideration. For active sonars this means the longest pulse length. For passive sonars, it means the longest observation time possible before the detection decision is made.

In active sonars, the maximum allowable pulse length is usually determined by the emergence of reverberation as the background that masks the echo; therefore, no increase in echo-to-reverberation ratio is obtained by an increase in pulse length. The use of long pulses without a corresponding build-up of the coherent reverberation background is achieved in sonars using pseudo-random noise for transmission and clipped time-compressed correlators for reception. Such sonars are useful against reverberation backgrounds or against targets of low doppler shift.

The reverberation background is a noise component unique to the active sonar environment. The auditory detection threshold is seriously constrained by the skill of a human operator. A more optimum detection system could be devised if the detection threshold was established by processing the output of a radiometric type sonar receiver. This is a switched

device wherein the input signal spectrum, including the reverberation background, is compared with a pseudo noise source (an independent sample of the reverberation background) to provide an optimum signal energy detector. A high speed A/D converter can be used to process sequential samples and the difference presented to a decision processor.

The spectrum of the reverberation is strictly a function of transmitting pulse width giving rise to the characteristic $[\sin X/X]^2$ power spectrum. The echo spectrum and the reverberation spectrum are virtually undistinguishable. The most effective way to alleviate this condition is to normalize the reverberation in the early stages of signal conditioning prior to actual signal detection. This normalizing process can be accomplished in several ways basically falling under the heading of open loop control and closed loop control. With the wide dynamic range reverberation input normalized, amplitude detection of the echo superimposed on the reverberation becomes feasible.

### 2.5.2 Postulated Future System Requirements

The high speed A/D converter can find numerous applications as a predetection quantizer in sophisticated signal processing sonar systems. The signal environment for sonar systems is extremely complex covering a wide frequency spectrum with signal to noise ratios encompassing a very wide dynamic range. Predetection processing of the receiver IF requires a high speed A/D converter designed to accommodate a very wide dynamic range. Particular and unique characteristics of the amplitude infrastructure contains information about the character of the target and may be of interest to the processor. The time history of the duration of the echo may contain information relating to the physical size and current aspect of the target.

To provide a reference against which to measure target doppler, a continual monitoring of the frequency content of the acoustic reflections is required. All incoming frequency variations other than that due to target motion must be sensed and normalized to provide an "own Doppler" frequency reference which can be used to measure accurately the amount of target doppler.

Input signals can be directly sampled at carrier frequencies and converted to digital signals for subsequent processing using any of the

frequency domain analyses techniques such as the fast Fourier transform (FFT) or the ultra-fast Fourier transform (UFT).

In a typical high resolution sonar application, 100 kHz sonar signals are processed for identification and direction finding. A linear array using 128 hydrophones provide input signals for transformation and integration. All 128 input signals are sampled simultaneously and transformed into the frequency-domain with the FFT processor. The use of simultaneous encoding of a multiplicity of sensors implies a need for a large number of low cost, high speed digitizers designed to satisfy the sonar system performance requirements.

# 3. A/D TECHNOLOGY STUDY

High speed A/D converters can be built using several different electronic device technologies. Existing state-of-the art A/D converters use silicon bipolar transistors. Future advances in circuits, algorithms, and processing will increase the performance of future silicon A/D converters. Several newer solid state technologies, including galium arsenide FETs, galium arsenide TEDs, and Josephson junctions, appear to offer the potential for advanced A/D converters with higher speed and less power than will ever be possible with silicon bipolar transistors.

Potential also exists in the electro-optic technologies employing either electron beam or laser beam devices. The following sections discuss the existing A/D converter state-of-the-art and future potential of each technology.

## 3.1 SILICON BIPOLAR TECHNOLOGY

Significant performance improvements in high speed A/D converters have been realized with the development of silicon bipolar LSI technology. Single chip monolithic quantizers are now available which offer orders of magnitude improvement in cost, parts count, and power consumption over previous discrete and hybrid units, while simultaneously improving speed and accuracy. The maturity and reliability of the silicon bipolar process make it currently the only LSI technology available for high speed A/D converter applications. The state-of-the-art in silicon bipolar processing is far from reaching its limits of maximum performance, and will soon complete with other technologies (e.g., GaAs FET) that offer the potential for much higher speeds. This section will discuss the current capabilities of the silicon bipolar technology and its potential for future development.

### 3.1.1 Device Characteristics

A figure of merit for characterizing the high frequency performance of bipolar transistors is the common emitter unity current gain frequency, $f_T$.

Considerable insight into the fundamental speed limitations of silicon bipolar devices and the potential for performance improvement can be gained by examining the equation for $f_T$. Basically, $f_T$ is related to the physical structure of the transistor through the emitter-to-collector delay time, $\tau_{EC}$, by

$$f_T = \frac{1}{2\pi\tau_{EC}}$$

Delay time $\tau_{EC}$ is the sum of five time constants,

$$\tau_{EC} = \tau_e + \tau_b + \tau_d + \tau_c + \tau_s.$$

Emitter depletion layer charging time $\tau_e$ is equal to the time constant formed by the dynamic resistance of base-emitter junction $r_e$ and base-emitter junction capacitance $C_{TE}$,

$$\tau_e = r_e C_{TE} = \frac{kT}{qI_E} (C_{TE}).$$

where

$k$ = Boltzman's constant

$T$ = temperature in $^oK$

$q$ = electron charge

$I_E$ = quiescent emitter current.

Base transit time constant $\tau_\beta$ is defined as the time required for the minority carriers to traverse the base and is approximately proportional to the square of the base width.

The third contributor to the emitter-collector delay time is collector-base depletion layer transit time $\tau_d$ and is given by

$$\tau_d = \frac{x_d}{2V_{sc}}$$

where

$x_d$ = depletion layer width

$V_{sc}$ = scattering-limited drift velocity in the collector ($\sim 8.5 \times 10^6$ cm/sec)

The fourth contributor is collector charging time constant $\tau_c$ which is equal to the time constant formed by collector series bulk resistance $r_c$ and collector-base junction capacitance $C_{cb}$:

$$\tau_c = r_c C_{cb}.$$

Final time constant $\tau_s$ is formed by the collector series bulk resistance $r_c$ and collector-substrate capacitance $C_{cs}$:

$$\tau_s = r_c C_{cs}.$$

For a typical silicon bipolar transistor, approximately half of the total emitter-to-collector delay time is due to base transit time $\tau_b$. Therefore, one of the basic limitations of the silicon bipolar technology is the ability to produce very narrow base widths. Current advanced LSI processing techniques produce base widths on the order of 1000 Å. However, discrete microwave bipolar transistors reportedly have base widths on the order of 500 Å. If a 2:1 reduction in base width could be achieved while maintaining LSI yields, a significant speed improvement (approximately 33 percent assuming no changes in the other time constants) can be realized. Although this requires the ability to produce very shallow diffusions in a controllable and reliable manner, it is not beyond the realm of present technological ability.

The second fundamental limitation of silicon bipolar transistor speed is the parasitic junction capacitances. A significant improvement in this area can only be realized by shrinking the transistor geometry. This is presently limited by the resolution of the photolithographic process. The use of advanced lithographic techniques, such as electron-beam lithography, can allow a factor-of-four reduction in linear dimensions. This would imply over an order-of-magnitude reduction in device area and thus a corresponding reduction in device capacitance. However, since the maximum current handling capability of the transistor is also reduced, no decrease in emitter depletion layer charging time $\tau_e$ is expected (although power consumption is reduced significantly). However, the two collector charging time constants, $\tau_c$ and $\tau_s$, will be reduced substantially. If improved lithographic techniques cause a 10:1 reduction in $\tau_c$ and $\tau_s$, and advanced

process control causes a 2:1 reduction in base transit time, a factor of two improvement in $f_T$ should be realized. Thus, the silicon bipolar technology has the potential of producing 8 to 12 GHz transistors with LSI yields. Present and future LSI bipolar transistors are compared in Table 3-1.

Table 3-1. LSI Bipolar Transistors

| | PRESENT STATE OF ART | FUTURE DEVICE | UNITS |
|---|---|---|---|
| $f_t$ | 3 → 5 | 8 → 12 | GHZ |
| $C_{bc}$ | 0.14 | 0.014 | pf |
| $C_{cs}$ | 0.16 | 0.016 | pf |
| $I_{c\ MAX}$ | 2 | 0.2 | MA |

### 3.1.2 Silicon Bipolar General Circuit Capabilities

The high speed of bipolar transistor logic is best exemplified by emitter-coupled logic (ECL). There are several variations of ECL: Motorola MECL III, Fairchild 100K, and TRW differential emitter coupled (DECL). The best commercially available ECL logic gates today have delays of about 750 psec, with 40 mW, power per gate for MSI devices. The most advanced high speed capability of silicon bipolar transistors is demonstrated through custom circuits with complexity greater than MSI. Gate delays in the 300 to 400 psec range have been achieved in single gate and LSI complexity. Silicon bipolar flip-flops are compared in Table 3-2. The TRW process is used for custom LSI development, while the other processes are used for commercial production.

Table 3-2. Comparison of High Speed ECL Flip-Flops

| MANUFACTURER | PART NO. | MAXIMUM TOGGLE RATE (GHZ) | POWER (MW) |
|---|---|---|---|
| TRW | OAT D F/F | 1.4 | 150 |
| FAIRCHILD | 11C06 | 0.75 | 200 |
| MOTOROLA | MC1690 | 0.5 | 200 |
| PLESSEY | SP1690B | 0.5 | 200 |

A fundamental building block in all A/D converters is the analog comparator. Realizing that a comparator has to be fast for both large and small input signals, high speed comparators use the strobed comparator circuit. Current silicon bipolar strobed comparators are capable of 0.1 mV accuracy over a 2 volt input range with a decision rate of greater than 100 Msps and a power consumption of less than 50 mW. Comparator delay time of approximately 2 nsec can be achieved.

The three circuit building blocks discussed in this section demonstrate that circuit techniques do exist which make maximum use of the performance potential of the silicon bipolar technology. While circuit development is a continual process, any advancement in the processing technology itself will produce a significant increase in circuit performance.

### 3.1.3 A/D Converter Organizations

A number of A/D conversion algorithms or organizations can be applied to the design of high speed A/D converters. Selecting the optimum organization depends on the speed, resolution, and power requirements for a given application. In general, four types of A/D organizations are best suited for high speed applications:

1) Successive approximation (SA)

2) Series-parallel feedback (SPFB)

3) Series-parallel feedforward (SPFF)

4) All-parallel.

This section will briefly describe each organization and present an estimate of current maximum performance capabilities for each type.

### 3.1.3.1 Successive Approximation A/D Organization

A block diagram for an N bit successive approximation A/D converter organization is shown in Figure 3-1. This approach employs a sample and hold, comparator, an N bit register with conversion logic, a digital-to-analog (D/A) converter, a dc reference circuit, timing, and an output register.

At the start of the conversion sequence the S/H circuit samples the analog input signal, and all latches in the N bit register, except the one for the most significant bit (MSB), are set false. The MSB is set true so that the D/A converter provides a voltage equal to one-half of full scale. This voltage is compared with the output of the S/H. If the S/H output is larger, the latch for the MSB remains in the positive state; if not it is set false. Simultaneously, the latch for the second MSB is set true. This process is repeated until all N bits have been determined.

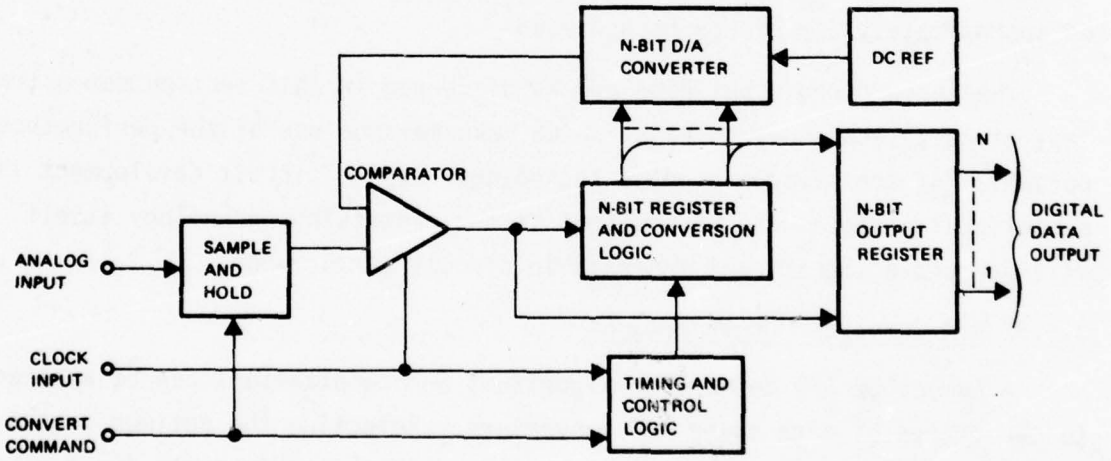



Figure 3-1. Successive Approximation A/D Organization

The successive approximation organization is the simplest converter configuration and has the fewest error sources. However, since the N bits are determined sequentially, this is the slowest high speed A/D converter organization.

The current state of the art in high accuracy (N≥ 8 bits), 1 bit/cycle successive approximation A/D converters, is being set by TRW single chip monolithic converters. The time/cycle is 8 to 12 nsec on existing converters. Current S/H circuits require one or two extra conversion cycles to acquire and settle to the required accuracy. Therefore, N bit successive approximation A/D converters required N +1 or N +2 cycles/conversion. Cycle times of 8 nsec for high accuracy converters are at the limit of present silicon monolithic technology. This limitation sets the upper bound on successive approximation conversion rate at about 14 Msps for an 8 bit, 9 cycle A/D (one extra cycle for the S/H).

3.1.3.2 Serial-Parallel Feedback A/D Organization

A block diagram for the serial-parallel feedback (SPFB) approach to A/D conversion is shown in Figure 3-2. For an N bit conversion this approach uses a Q bit quantizer N ÷ Q times duing the conversion period to generate the required N bits. An N - Q bit D/A and quantizer reference circuit provide the proper reference voltages to the $2^Q$ - 1 comparators in the Q bit quantizer. The analog input to the quantizer comes from the output of the S/H circuit. The voltage at this point remains constant during the entire conversion period.

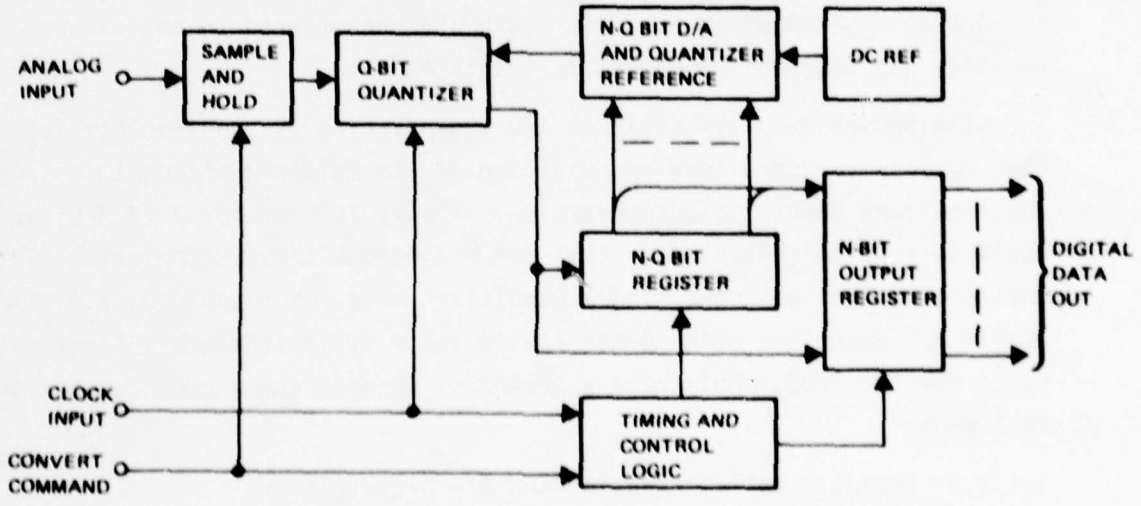



Figure 3-2. Serial-Parallel Feedback A/D Organization

The conversion period is divided into N ÷ Q cycles by the timing logic. It is often necessary to provide an additional cycle to allow the S/H circuit adequate time to acquire and track the analog input signal. The first cycle begins by sampling the analog input and then holding this sampled value until the start of the next conversion period. Throughout the first cycle the A/D control logic spreads the reference voltages to the individual comparators in the quantizer uniformly over the full voltage range of the A/D converter. At the end of the first cycle, the comparators are strobed and the Q bit digital outputs are the MSBS of the conversion. These MSBS are fed back to the D/A and quantizer reference circuits to position the comparator references for the second cycle of the conversion period. The comparator reference voltage sequence for a SPFB (3,3,3) converter is shown in Figure 3-3.

During the second cycle, the comparator references are spread uniformly over $2^{-Q}$ of the full voltage range of the A/D. The thresholds of the quantizer are now equally spaced within the one step determined at the end of the first cycle. At the end of the second cycle, the comparators are strobed again, and Q more bits of the N bit result are determined. This process continues until all N ÷ Q cycles have been performed. At the end of the last cycle, the N - Q bits determined in preceding cycles and the Q bits determined in the last cycle are transferred to the output register and another conversion is initiated.

The series-parallel feedback A/D organization is considerably faster than successive approximation by virtue of its multiple bit decisions/cycle and resultant fewer cycles/conversion. The cycle time for 2 to 5 bits/cycle would only be slightly longer that for a single bit/cycle converter if the entire quantizer was on a single monolithic chip. For example, a 4 bit/cycle 12 bit A/D quantizer with 15 nsec/cycle and 4 cycles/conversion (one extra cycle for the S/H), would have a period of 60 nsec and a conversion rate of 16.7 msps.

### 3.1.3.3 Serial-Parallel Feed-Forward A/D Organizations

The general class of A/D converters, falling into the serial-parallel feed-forward (SPFF) category, employs a bank of $2^{Q} - 1$ comparators which determine the most significant Q bits of an N bit A/D conversion. This is followed by one or more similar banks of comparactors which determine the

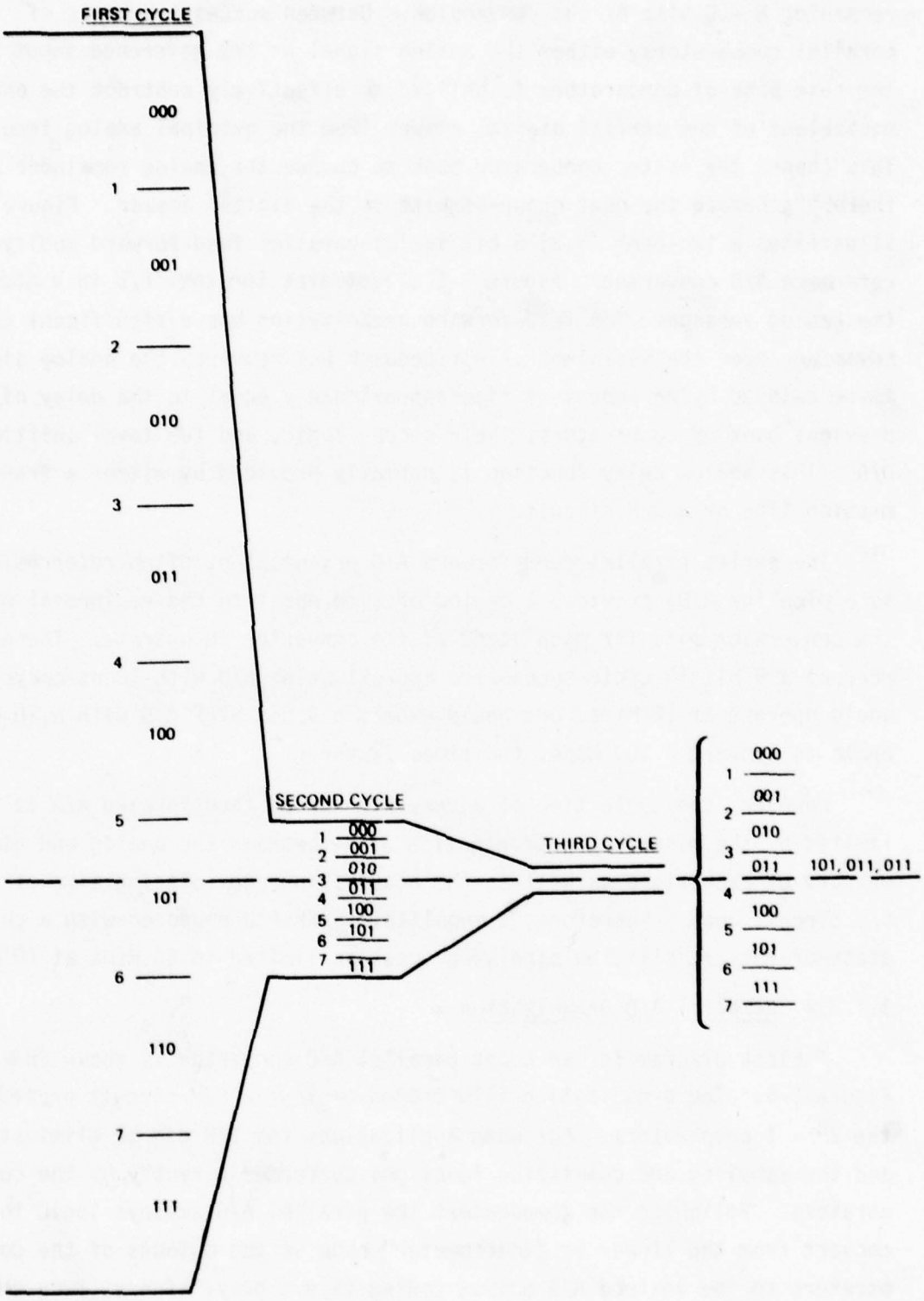



Figure 3-3. Comparator Reference Spreading for 3,3,3 SPFB A/D

remaining N - Q bits of the conversion. Between successive banks of parallel comparators, either the analog signal or the reference input to the next bank of comparators is shifted to effectively subtract the analog equivalent of the partial digital answer from the original analog input. This causes the latter comparator bank to encode the analog remainder and thereby generate the next group of bits in the digital answer. Figure 3-4. illustrates a two-bank (3,3) 6 bit serial-parallel feed-forward modify-the-reference A/D converter. Figure 3-5 illustrates the same A/D in a modify-the analog version. The feed-forward organization has a significant speed advantage over the serial-parallel feedback but requires the analog signal to be delayed by an amount of time approximately equal to the delay of the previous bank of comparators, their decode logic, and the level shifting D/A. This analog delay function is normally provided by either a transmission line or a S/H circuit.

The series-parallel feed-forward A/D organiation, often referred to as a pipeline A/D, provides a period of time equal to the reciprocal of the conversion rate for each stage of the converter to operate. Therefore, whereas a 9 bit 10 cycle successive approximation A/D with 10 nsec/cycle would operate at 10 Msps, one would expect a 9 bit SPFF A/D with a 10 nsec cycle to convert a 100 Msps, ten times faster.

However, the cycle time of a very high speed feed-forward A/D is often limited by the mismatch in propagation delay between the analog and digital outputs of each stage as well as the acquisition and settling time of the S/H circuit used. Therefore, a monolithic SPFF A/D produced with a current state-of-the-art silicion bipolar process is limited to 60 Msps at 10 bits.

3.1.3.4 Parallel A/D Organization

A block diagram for an N bit parallel A/D converter is shown in Figure 3-6. The organization illustrated employs a S/H circuit preceding the $2^N$ - 1 comparators. For some applications the S/H can be eliminated and the sampling and quantizing functions performed directly by the comparators. Following the comparators the parallel A/D employs logic to convert from the linear or "thermometer" code at the outputs of the comparators to the desired A/D output coding (i.e., gray, binary, twos complement, etc.). Each data word is strobed into the output register. Timing

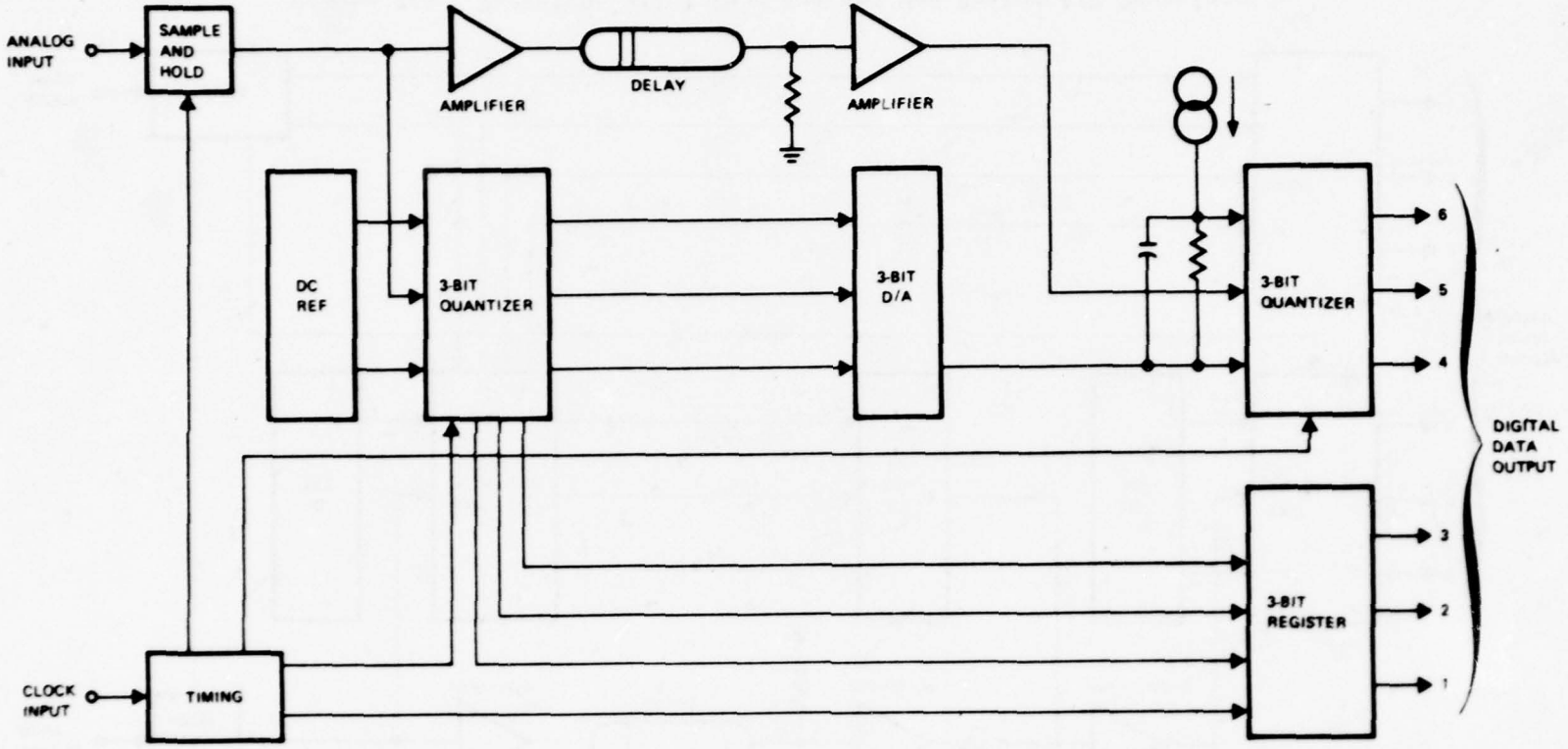



Figure 3-4. Serial-Parallel Feed Forward Modify Reference A/D Organization

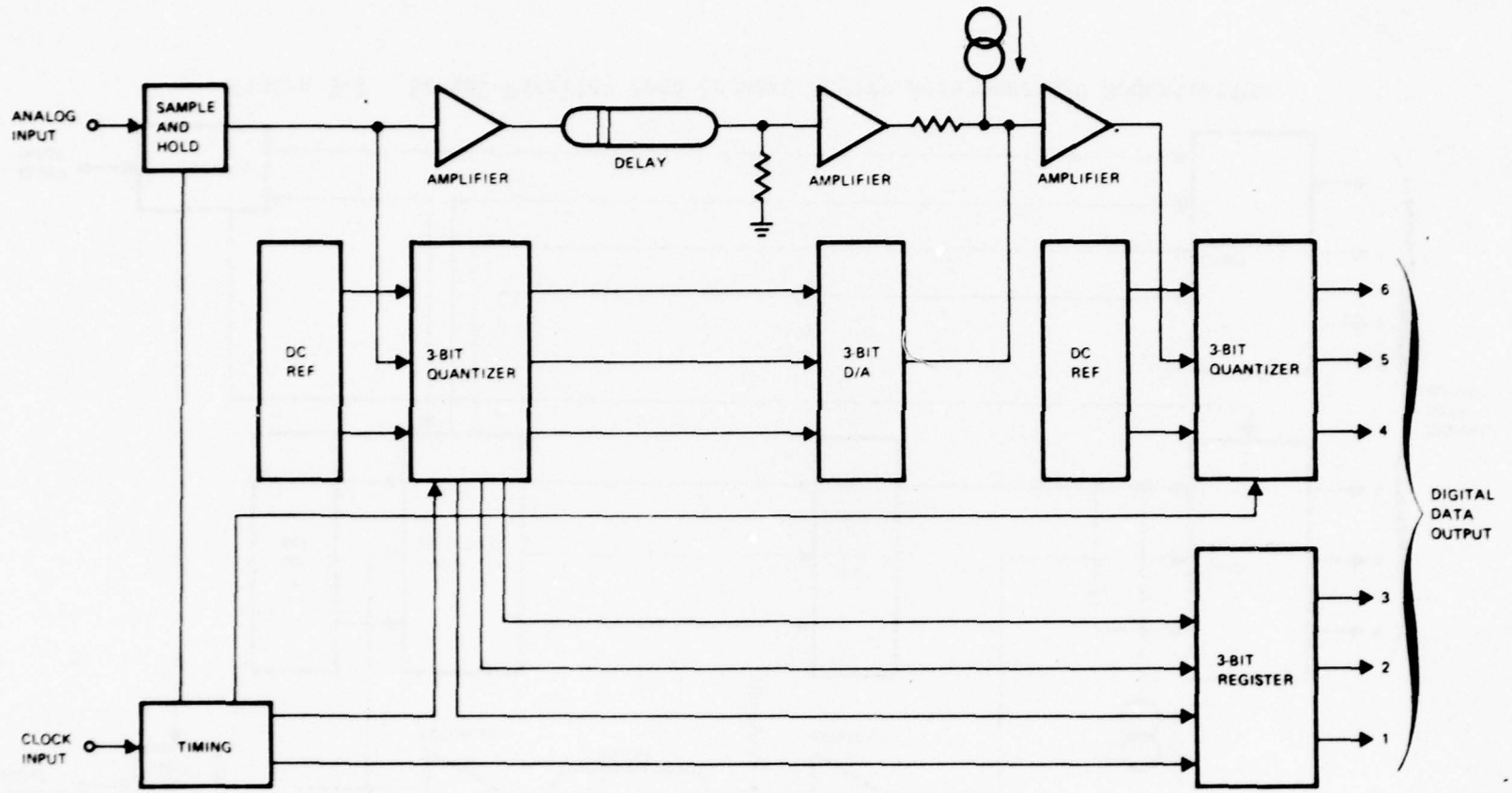



Figure 3-5. Serial-Parallel Feed Forward Mod Analog A/D Organization

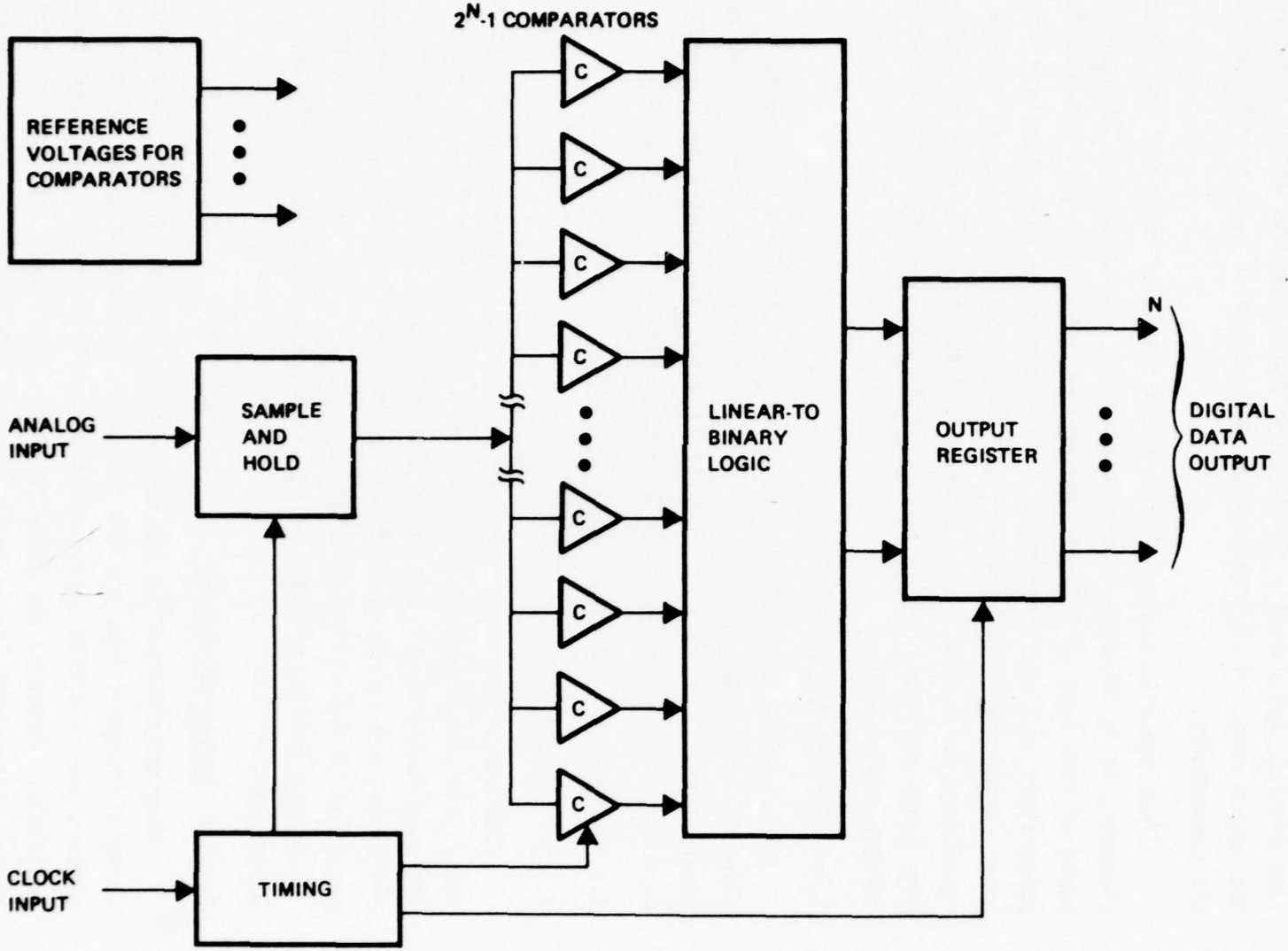



Figure 3-6. N Bit Parallel A/D Organization

circuits operate the S/H, comparators, and output register in the proper time phasing, and output a timing pulse (data-ready pulse) in-phase with the output code. A reference generator provides a voltage reference for all comparators.

Since the all-parallel A/D contains the least number of serial delay elements, it is potentially the fastest A/D organization. The major drawbacks of this type of A/D are limited resolution (due to limited number of comparators that can be produced on a single monolithic chip) and high power consumption. With current processing capabilities, the maximum resolution for a single chip all-parallel A/D is 6 bits with a sampling rate about 100 Msps. Using multiple chips, higher resolution A/D converters can be built.

### 3.1.4 Present A/D Capabilities

The present state of the art in silicon bipolar A/D converters is given in Table 3-3. Where the listing is for a quantizer, the LSI quantizer listed requires a S/H circuit (1 watt) plus timing and interface circuitry ranging from zero to 2 watts depending on application.

### 3.1.5 Limits of Associated Analog Functions

#### 3.1.5.1 Sample and Hold

The successful development of low power, high speed, high resolution, monolithic quantizers has made present thin film hybrid S/H circuits the limiting factor in A/D economics and reliability. The development of a monolithic S/H is required to realize the full low cost, high performance potential of the silicon bipolar technology. This development will ultimately lead to single chip monolithic A/D converters (S/H plus quantizer).

#### 3.1.5.2 Analog Multiplexer

Many multichannel system applications require analog multiplexing of serveral channels into one A/D converter. Present high accuracy multiplexers use thin film hybrid construction to achieve good linearity and crosstalk. However, the moderate speed, high power, and high cost of these multiplexers limits their range of applications. The development of

Table 3-3. Present State of the Art in Silicon Bipolar A/D Converters

| SAMPLE RATE (MSPS) | BITS | POWER (WATTS) | ORGANIZATION | STATUS | COMPANY | COMMENTS |
|---|---|---|---|---|---|---|
| 2 | 12 | 1.7 | SA | DEVELOPMENT COMPLETE | TRW | SINGLE CHIP LSI QUANTIZER |
| 5 | 10 | 2.9 | SA | IN PRODUCTION | TRW | SINGLE CHIP LSI QUANTIZER |
| 7 | 8 | 2.4 | SA | IN PRODUCTION | TRW | SINGLE CHIP LSI QUANTIZER |
| 10 | 10 | 2.8 | SA | IN PRODUCTION | TRW | SINGLE CHIP LSI QUANTIZER |
| 12 | 8 | 0.8 | SA | DEVELOPMENT COMPLETE | TRW | SINGLE CHIP LSI QUANTIZER |
| 20 | 8 | 2.6 | SPFB | DEVELOPMENT COMPLETE | TRW | SINGLE CHIP LSI QUANTIZER |
| 30 | 8 | 2.0 | PARALLEL | IN PRODUCTION | TRW | SINGLE CHIP LSI A/D CONVERTER |
| 50 | 10 | 2.5 | SPFB | IN DEVELOPMENT | TRW | COMPLETE A/D CONVERTER |
| 60 | 10 | ~25 | SPFF | DEVELOPMENT COMPLETE | HUGHES | COMPLETE A/D CONVERTER |
| 250 | 8 | 60 | PARALLEL | IN DEVELOPMENT | HUGHES | COMPLETE A/D CONVERTER |
| 400 | 5 | 20 | PARALLEL | DEVELOPMENT COMPLETE | TRW | COMPLETE A/D CONVERTER |

a monolithic analog multiplexer, is required to maintain compatibility with high performance monolithic A/D converters. TRW has developed an ultra-high speed monolithic five input analog multiplexer for a 5 bit, 400 Msps application and is currently developing a four input 25 Msps analog multiplexers for a low power 8 bit application.

### 3.1.6 Limits of Associated Digital Functions

A survey of currently available digital functions indicates that their performance is compatible with existing A/D converter hardware. Table 3-4 lists some of the high speed digital functions frequently required in signal processing systems. Note that these elements will accept data at rates provided by current high speed A/D converters. However, considerable savings in parts count and power could be realized through the use of a custom LSI design. The available packing density of current state-of-the-art silicon bipolar designs is the limiting factor in determining the maximum number of digital functions that can be integrated on a single LSI chip. The maximum device count for present high speed silicon bipolar processes depends on layout efficiency but have a practical yield limit (based upon minimum device size) of approximately 4000 to 5000 devices. Future processing technologies which allow higher circuit complexity will provide a substantial costs reduction in high volume digital processing hardware.

### 3.1.7 Summary of Future Potential of Silicon Bipolar Technology

Using current state-of-the-art silicon bipolar technology, single chip monolithic quantizers with output data rates ranging from 50 Mbps to 1 Gbps are realizable. The development of a monolithic S/H and advanced quantizer circuits will make low power, single-chip A/D converters a reality. Future performance improvements will come in the form of high resolution (electron-beam) lithography and highly controlled shallow diffusion processes. These developments will double the maximum sampling rate with a significant reduction in power consumption, as well as improve device matching (which is a major contributor to A/D level errors). The immediate development of electron-beam lithography and tighter process controls will not only provide near-term advances in silicon bipolar technology but can also be applied to future technologies

Table 3-4. Associated Digital Functions

| FUNCTION | TECHNOLOGY | SPEED (NSEC) |
|---|---|---|
| 1 K RAM | FAIRCHILD ISOPLANAR ECL (SI BIPOLAR) | 20 |
| 1 K ROM | FAIRCHILD ISOPLANAR ECL | 15 |
| 8-INPUT DIGITAL MULTIPLEXER | FAIRCHILD ISOPLANAR ECL | 2 |
| 4-BIT ALU | FAIRCHILD ISOPLANAR ECL | 5 |
| 4 X 4 MULTIPLER | TRW OAT ECL | 10 |
| 8 X 8 MULTIPLER | TRW OAT ECL | 15 |

(such as GaAs FET) as well. As the requirement for higher speed digital processing increases, the need for such processing developments becomes more evident. On the circuit design level, continuing efforts to update the associated analog and digital functions will ensure additional growth of state-of-the-art A/D converters.

## 3.2 GALLIUM ARSENIDE FET TECHNOLOGY

### 3.2.1 Technology Description

Being a new technology, GaAs FET IC processes are not as mature as those for silicon IC. Extensive research and development efforts are currently being spent on GaAs FET processes because of the low power, high speed potential. Presently, several different GaAs FET processes are capable of fabricating SSI and MSI circuits with reasonable yield and can be differentiated by their active devices and processing methods. Three basic steps in GaAs FET processing are: substrate preparation, active layer formation, and isolation. Within each basic processing step are two or three options (Figure 3-7). Utilizing different options at different steps, a variety of GaAs IC circuit elements can be generated. In the active device category are Schottky diodes, n-channel depletion mode MESFET, n-channel enhancement mode MESFET, and n-channel enchancement mode JFET. To complement these active devices, these processes can also fabricate different resistors and capacitors. The common passive components are bulk resistors, implant resistors, metal-film resistors, and MOS capacitors. A metal-interconnect system, is used to interconnect these devices into useful circuits. Recent U.S. success in GaAs IC fabrication has been reported by Hewlett-Packard Laboratories, McDonnell Douglas Astronautics Company, Rockwell International Science Center, and TRW Defense and Space Systems Group. State-of-the-art GaAs IC FET processes today are capable of fabricating small geometry GaAs FETs with gate length down to one micron and channel depth equal to a few thousand angstroms. The characteristics of such a FET are:

- Pinch-off voltage: $Vp = \sim I\ V$
- Saturated drain current: $I_{DSS} \sim 80\ \mu A/\square$
- Transconductance at saturation: $g_{mo} \sim 80\ \mu mhos/\square$
- Gate input capacitance: $C_G \sim 1.5\ ff/(\mu m)^2$
- Source resistance: $R_S \sim 100\Omega$
- $V_{GS}$ match between adjacent FETS: 20 mV
- $I_{DSS}$ match between adjacent FETS: 2.4$\mu$A/ ;

$\square$ is defined as the ratio of gate width/gate length.

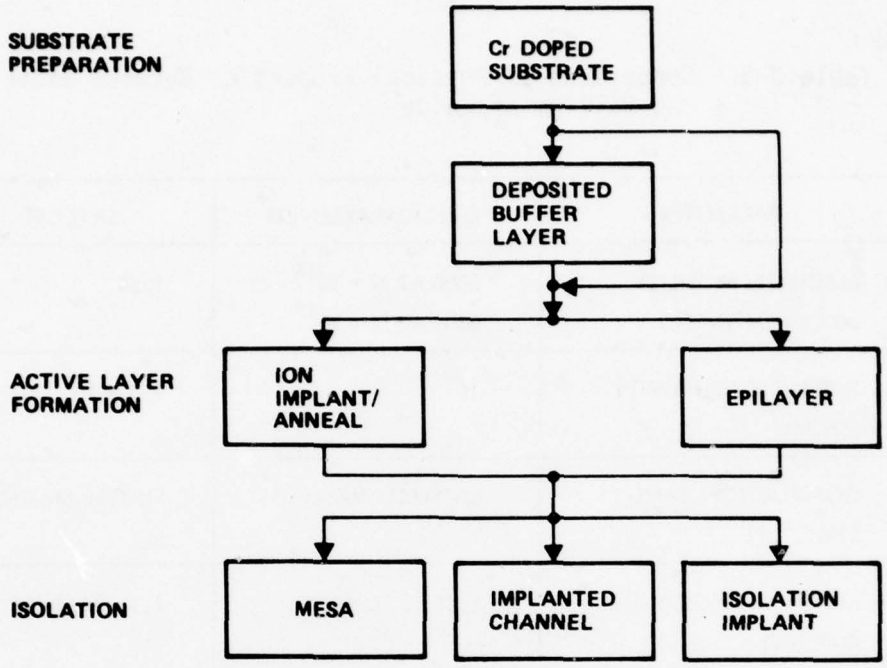



Figure 3-7. *GaAs FET Processing*

The complexity of these GaAs FET circuits is presently SSI level, including such functions as frequency divider, BPSK modulator, wideband linear amplifier, and transistor arrays. Maximum circuit operational frequency in the range of 1 to 5 GHz with power consumption ranging from a few milliwatts to hundreds of milliwatts has been achieved.

Since GaAs FET IC technology is still developing, the existing fabricated circuits and device characteristics are not representative of the technologies potential. The following accessment of GaAs FET technology is performed according to various fundamental physical properties of GaAs material, and intrinsic characteristics of a FET. Several aspects of the processing technique are also discussed.

3.2.1.1 GaAs Material

A comparison of silicon and GaAs physical properties that affect the overall performance of an active IC device is shown in Table 3-5.

Table 3-5. Comparison of Physical Properties Between Silicon and Gallium Arsenide

| PARAMETER | GALLIUM ARSENIDE | SILICON |
|---|---|---|
| ELECTRON MOBILITY 300°K ($CM^2/VSEC$) | 3000 AT N = $10^{18}$<br>8500 AT N = $10^{15}$ | 1350 |
| INTRINSIC RESISTIVITY ($\Omega CM$) | $10^8$ | $2.5 \times 10^5$ |
| CONDUCTION BAND STRUCTURE | SATELLITE VALLEYS | SINGLE MINIMUM |
| MINIMUM ENERGY GAP (EV) | 1.35 EV, DIRECT | 1.11 EV, INDIRECT |
| THERMAL CONDUCTIVITY (WATTS/$CM^\circ K$) | 0.44 | 1.42 |

The high field mobility of electrons in GaAs is one of its greatest attributes. This relatively high mobility leads to higher frequency operations of various active devices especially field-effect transistors. Due to extremely short minority carrier lifetime, it is impractical to fabricate a bipolar GaAs transistor. For these reasons most of the GaAs technologies are oriented toward FET processing. Furthermore, GaAs high intrinsic resistivity provides good isolation between adjacent circuit elements as well as minimum parasitic capacitance. Thus, GaAs is an ideal substrate material for a monolithic IC process.

Another striking differences between gallium arsenide and silicon are due to dissimilarities in band structure. The band gap of GaAs is 1.35 eV, while that of Si is 1.11 eV. More subtle are the differences due to the conduction band minima postions with respect to the valence band maxima. The valence-to-conduction-band transition in Si is indirect, and therefore involves a three-body collision, a process which seldom occurs due to the probabilities involved. GaAs, on the other hand, has a direct transition which involves only a two-body collision process, and

thus minority carrier lifetimes are reduced over those of silicon by orders of magnitude. Combining with a larger bandgap, GaAs has larger radiation hardness than Si. Yet a third variant is the structure of the conduction band; GaAs has the satellite valleys which, when coupled with the mobilities and densities of states of the two conduction band minima, lead to the transferred electron effect. This effect gives rise not only to a very broadband negative resistance, but also to an extremely fast switching mechanism that forms the basis of high speed switching for TED logic.

A disadvantage of GaAs in comparison with silicon is its thermal conductivity (see Table 3-5). Thermal considerations are important in the design and fabrication of integrated circuit, particularly in LSI. Power dissipation of a GaAs IC can become a dominant constraint on the size and complexity of the circuit.

3.2.1.2 FET as Baseline Active Device

The most distinctive difference between a FET and a BJT is that the FET uses majority carriers for current transport. Using majority carriers for conduction, the FET is practically free of storage effects, and therefore has shorter propagation delay. The voltage control mechanism in the FET provides a high input gate impedance, which is desirable in many circuits.

Most GaAs FET IC technologies are working toward micron or submicron FET geometries to maximize the transconductance-to-capacitance ratio and produce high speed, low power circuits. However, these small devices produce GaAs FET circuits in which speed performance is very sensitive to the parasitic capacitance and, especially the load capacitances resulting in the need for output buffers to drive typical package and interconnect impedances.

3.2.1.3 Processing Techniques

In the course of GaAs FET fabrication, a number of important processing considerations determine the performance of the resultant FET. These are briefly discussed below.

Characterization of the GaAs material is essential during the course of processing. An accurate characterization can identify a potential low-yield wafer and allow compensating action to be taken. Different characterization technique are available today. They include Hall measurements, concentration profiling by capacitance-voltage methods, surface examination, thickness measurements, current injection measurements, and semiconductor junction profiling by measurement of Anger electron peak shifts in a scanning electron microscope.

Precision lithography is another important aspect particularly for small geometry FET. Small geometry FETs have very little tolerance in mask alignment and lateral variations. Advanced optical equipment, like a Cannon 4X projection mask aligner, is normally employed; E-beam techniques are also being used.

Active channel formation is a crucial step for a successful FET device. In this step, the controllability of the channel depth and concentration have been difficult because of the precision required. Active channels are currently being formed by epitaxial growth and ion implanation. Ion-implant techniques give better controllability but greater crystal defects if post-annealing is not applied properly. This technique also provides a possibility of multiple selective implant into selected regions.

Isolation is very important in integrated circuit fabrications. Several isolation techniques are available: mesa etch, active channel implant, and isolation implant. Among them, the active channel implant is the most desirable because it is a planar process and has better dimensional control and better isolation when compared to the alternate techniques.

Metallization is another important processing step. It is employed to fabricate FET gates, ohmic contacts, and interconnections. Selection of proper metal, deposition temperatures, and concentration in the contact region are required for successful metallization.

### 3.2.2. GaAs FET Application in A/D Converter Circuits

Gallium arsenide FETs have a number of distinct features that enhance the performance of A/D subcircuits:

- Low parasitic capacitances
- High input impedance
- Ability to make current sources and sinks
- Radiation hardness.

GaAs FET low parasitic capacitance provides considerably smaller nodal RC time constants in comparison with silicon bipolar. Lower bias current levels are required to achieve the same slew-rate requirements. Smaller RC time constant and lower current level imply higher speed and lower power, a prerequisite for high performance A/D converters.

The high input impedance of a FET has useful application as a high input impedance buffer in many A/D circuits, in particular the S/H circuit. For a simple illustration, a simplified S/H schematic is shown in Figure 3-8. An important S/H performance parameter, hold droop, is given by the following expression:

$$\text{Droop} = \frac{\Delta V}{\Delta t} = \frac{V_H}{RC}$$

where

C = hold capacitor

$V_H$ = instanteous hold voltage across R

R = input impedance

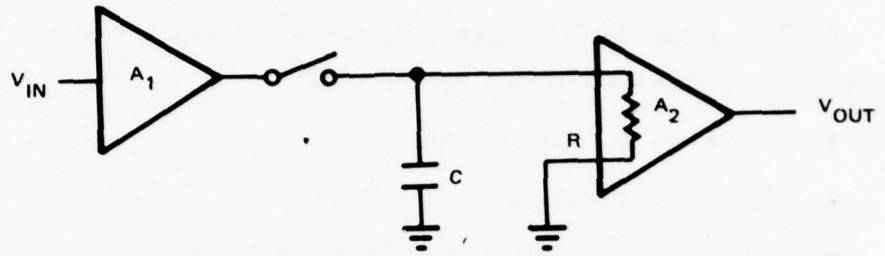



Figure 3-8. Simplified Sample-and-Hold

From the expression, it is obvious that the higher the input impedance, the smaller the droop. Smaller droop implies longer hold time and less hold error. High input impedance FET buffers can also be applied to circuits that are sensitive to current drain, like the comparator. A FET buffer can also be used in digital logic gates to increase the gate fanout and driving capability.

Another useful feature of a depletion-mode FET is that it can be used as both a current sink and current source. This capability is very useful in A/D converter circuit design. For example, a high-gain operational amplifier is difficult to achieve in a high speed bipolar transistor process lacking PNP devices because of the need for current sources. The unique FET capability of making current sources and sinks makes high-gain operational amplifiers very simple in a GaAs process. Besides the operational amplifier, novel S/H sampling gates, D/A converters, latches, and other useful circuits can be implemented easily with the current sink and sources capability of GaAs FET.

Radiation hardness is often a requirement in designing high performance A/D converters. In an A/D converter, the circuits that are most sensitive to radiation are the S/H, comparators, and D/A. If they are built with bipolar transistors these circuits will upset during x-ray exposure because of photo-current generation. Since GaAs FETs are majority carrier devices and have extremely short minority carrier lifetime, their electrical functions are not affected by photo-current generation – minority carrier effect.

GaAs FET devices have limitations that can degrade circuit performance if not properly considered. These characteristics are:

- High output impedance
- Device mismatches
- Temperature dependence of gate leakage current

High FET output impedance results from low FET gm. This leads to higher RC time constants which degrade the speed performance of a circuit having a large capacitive load.

Device mismatch and tracking are the principal error sources in analog circuits. For an A/D converter the most critical matching requirements occur in the comparator and the D/A circuits. FET gate-source voltage match and tracking errors will be manifested as nonlinearities for the A/D converter. Drift or offset error can degrade the accuracy of an A/D converter and the degradation will be determined by the LSB size of that A/D. Laser trimming of resistor values has been employed very successfully in silicon monolithic A/D converters to adjust initial match errors and is expected to be equally useful in GaAs circuits.

The present capabilities for resistor and FET device matching is adequate for 6 bit A/D converters, projected in 2 to 3 years to be adequate for 8 bit A/D converters, and with laser trimming can be extended to 12 bit A/D converters.

Temperature dependence of gate leakage current affects performance principally in the S/H circuit. In a Schottky barrier gate FET, the gate leakage current will approximately double every 10°C. In other words, for a 66°C increase in temperature, the leakage current will increase by $\sim$100 times. Even though the leakage current of an FET at nominal temperature is negligible, the leakage at high temperature can be considerable.

### 3.2.3 A/D Converter Organizations and Performance Projections

The same four basic high speed A/D converter organizations discussed for silicon LSI implementation are applicable for GaAs FET LSI circuitry. Performance projections are based on photolithographic mask making and processing (2 micron device geometries), and present circuit concepts. Improvements in both areas can be expected over the next 3 to 5 years

resulting in speed and power improvements of from 2 to 4 for designs 5 years hence. Each of the four A/D organizations described in the silicon bipolar section discussed here include speed and power performance estimates.

3.2.3.1 Successive Approximation

A successive approximation A/D converter uses a single comparator and an n bit D/A converter in a feedback loop to determine the digital value of the analog input by a trial and error technique. The successive approximation A/D needs at least n cycles for an n bit conversion. This is, therefore, the slowest of the high speed A/D conversion schemes. During each cycle, the comparator circuit compares the analog input, held by the S/H, with the D/A output and makes corresponding bit decisions and updates the D/A. This negative feedback loop, consisting of the D/A and comparator, forces the analog D/A output to become a successively closer approximation to the analog input as the conversion progresses. At the end of the conversion, this approximation will be within 1/2 an LSB of the input, and the digital result of the conversion will be equal to the D/A digital input. Performance of the successive approximation A/D converter is determined by the characteristics of the comparator and the D/A. A/D linearity is determined by the common mode rejection of the comparator and D/A converter linearity. Since only a single comparator is involved, the comparator's offset and drift error will manifest itself only as offset of the A/D converter. The successive approximation A/D has the best linearity, accuracy, and lowest part count and power consumption of the high speed A/D converter organizations. These advantages makes the successive approximation approach a very desirable algorithum for implementation in GaAs because it minimizes the FET match requirements, power consumption, and chip size.

A successive approximation A/D can achieve an accuracy of about 12 bits with only 150 mW power dissipation, and a conversion rate of about 50 Msps. The A/D will occupy an area of 60 x 80 mil.

### 3.2.3.2 Series-Parallel Feedback (SPFB)

This A/D organization is similar to successive approximation with the exception that two or more bits are decided in each cycle of the conversion. This allows the conversion to be completed in fewer cycles, resulting in substantially higher conversion rates at a slight increase in circuitry complexity and a decrease in the accuracy obtainable. The estimated speed of an 8 bit single chip SPFB complete A/D converter (including S/H and dc reference circuit) is 200 MHz at a total chip power of 200 mW.

### 3.2.3.3 Series-Parallel Feed-Forward (SPFF)

The SPFF organization is similar to the SPFB except that there is a separate bank of comparators for each group of bit decisions. This approach, which is a pipeline organization, further increases the converter circuitry and achieves a further increase in conversion rate if properly implemented. The estimated conversion rate of an 8 bit SPFF A/D (including S/H and dc reference circuit) is 300 MHz with a total A/D power of about 300 mW.

### 3.2.3.4 All-Parallel Approach

The all-parallel A/D converter organization is the fastest scheme of the four approaches being discussed.

The all-parallel approach uses $2^n-1$ comparators for an n bit A/D. An 8 bit converter therefore requires 255 comparators. Assuming 10 FETs per comparators, the device count of this A/D will be nearly 3000 FETs. Processing capabilities are expected to reach this level in 3 to 4 years.

A disadvantage of the all-parallel approach is the high power consumption. Due to the low thermal conductivity of GaAs, heat dissipation will impose a constraint on the upper bound of power consumption, which in turn limits the number of comparators that can be used and therefore the A/D resolution. Considering the above factors, the all-parallel approach is confined to medium accuracy A/D applications where the premium requirement is high sample rate.

The resolution of an all-parallel A/D will be limited by chip size and power to the range of 6 to 8 bits. This A/D is capable of performing conversion at a rate of 1 Gsps. The power and chip area of the A/D depends on the number of bits. For 6 bits, the A/D will have about 1800 devices on a chip about 85 x 85 mils. For 8 bits, the complexity will increase to about 7200 devices and an area of 170 x 170 mils.

### 3.2.4 Limitations of Associated Digital Functions

The high digital data rates produced by GaAs A/D converters will not pose an immanageable problem to successive digital functions such as multipliers, memories, or D/A converters since these functions can also be fabricated by the same GaAs process as is used for the A/D converter. A more detailed discussion of GaAs FET considerations for application to high speed, low power A/D converters and digital functions is given in Appendix A.

### 3.2.5 GaAs Process Development

Gallium Arsenide Technology is the most rapidly growing area in solid state circuits today. This technology was initially applied to Schottky barrier diodes, Gunn or transferred electron devices (TEDs) and avalanche transit time devices in RF microwave applications. The largest use of GaAs has been in light-emitting diodes until the most recent development of high performance FETs, gate-triggered TEDs and GaAs integrated circuits. The gate-triggered TEDs and FETs were developed initially as discrete devices, but have recently been fabricated in small scale integrated circuits. These are experimental monolithic circuits at several laboratories and are not presently available as commercial products. Extensive development is required in various areas to extend the integration level to a larger scale.

Ion implant technology requires additional development in the host material (Cr-doped substrate versus buffer layer), the implant species, implant conditions for achieving a specific doping profile, and annealing techniques. The resultant doping profile from ion implanations has been shown to be affected by these three processing parameters. Achieving the desired device parameters repeatedly requires better analysis and control of substrate materials or the use of a semi-insulating epitaxially-deposited buffer layer.

Ion implanted S, Se, and Si have been investigated in GaAs with Si being the most promising species for near ideal FETs. Predicting pinchoff voltage, i.e., the dopant concentration and penetration depth is dependent upon control of post implant annealing conditions. The primary concern has been the anneal temperature and the annealing caps. Additionally, the annealing caps must be compatible with subsequent device processing.

Ion implanted GaAs must be annealed at temperatures greater than 450$^{o}$C to activate the implanted species and in general heated to a temperature greater than 800$^{o}$C to remove the implant damage. When heated above 450$^{o}$C, GaAs dissociates at the surface yielding electrically active vacancies and in extreme cases shows surface eroding.

These conditions are alleviated by using an annealing cap or an arsenic overpressure (capless) during the annealing. It has been discovered that very low thermal time constant annealing can be achieved with E-beam or laser anneal. Development in this area will permit a more complete anneal without the concommitant diffusion. The capless anneal processes will simplify the photolithographic processing steps during circuit fabrication.

Development of submicron lithography techniques permit the fabrication of LSI circuits with about a micron gate and 1 to 2 micron dimensions. These small dimensions improve the device parameters as well as minimize interconnect parasitics. The maximum device speed is achieved by performing all functions on the chip and developing an optimum device to drive off of the chip. This may require development of different device types such as a heterojunction devices which would have to be made compatible with the other devices on the LSI.

## 3.3 GALLIUM ARSENIDE TED/FET TECHNOLOGY

### 3.3.1 TED/FET Technology Description

The transferred electron device (TED) is a candidate for performing general logic functions, primarily at clock rates above 5 Gbps. The transferred electron effect, which occurs in several semiconductor materials (most notably GaAs), involves the transfer of majority (electron) carriers to a higher energy (heavier) state in the bulk crystalline material at applied fields above a certain critical value $E_c$. For gallium arsenide at room temperature, $E_c$ is about 0.32 volt applied per micron of conducting channel length.

An oblique view of a typical TED imbedded in the surface of a multiple-TED monolithic-circuit GaAs chip is depicted in Figure 3-9. The implanted GaAs material is highly n-doped relative to the surrounding semi-insulating GaAs material and is shown dumbbell-shaped with the large ends covered with metal forming ohmic contacts to the implanted material. The active operating region is the straight channel between the two ohmic contacts. The gate metal is usually fabricated to form a Schottky diode contact with the active channel.

Typical TED active channel dimensions might be on the order of 1/2 micron for depth d, ten microns for width w, and length $l_{ca}$. The cathode is often grounded and the anode supplied with a positive bias voltage such that the channel field is slightly below the critical 0.32 volt/micron of channel length. Application of a small negative going voltage to the gate forces away (depletes) carrier electrons in the channel directly under the gate and thereby slightly reduces the effective cross-sectional area of the conducting channel under the gate. The field in this constricted part of the overall channel immediately rises above $E_c$, and the electrons in this constriction transfer to a high energy state in the implanted crystalline material. Normally, this effect is regenerative because as these heavy carrier electrons begin to drift relatively slowly (about 10 psec/micron at room temperature) toward the anode the relatively fast normal carrier electrons naturally pile up or accumulate on the cathode-facing side of the constriction. Meanwhile, the normal (more mobile) electrons on the anode facing side of the constriction quickly drift toward the anode, leaving a depletion region next to the constriction.

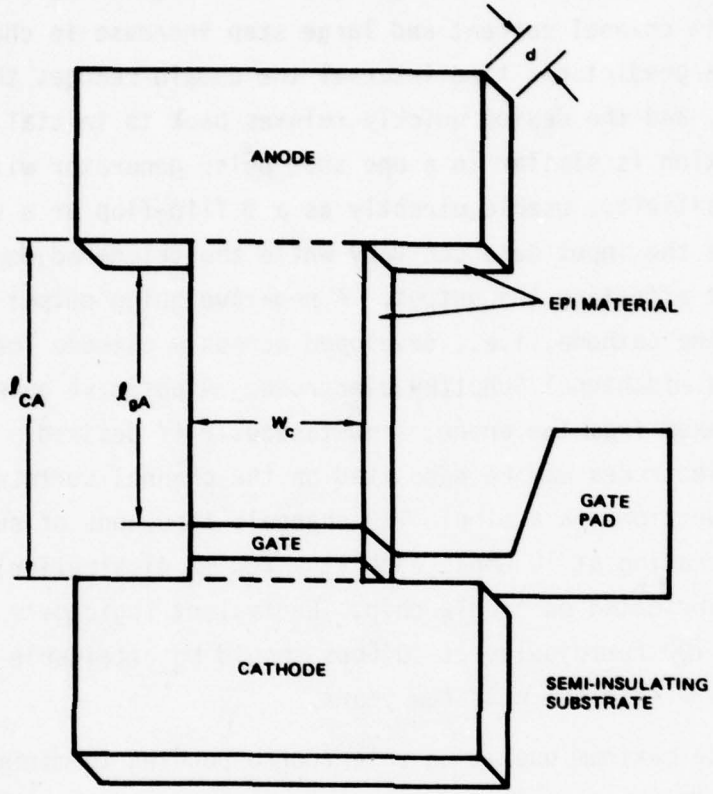



Figure 3-9. Gate Controlled TED Structure

Both effects (accumulation and depletion) increase the voltage gradient (field) across the constriction which in turn regeneratively increases the number of electrons transferring to the heavy state. Within a few psec the voltage across the accumulation-depletion space charge region (domain) can grow to about half the total channel voltage (i.e., applied anode voltage). The domain length, or total distance along the channel occupied by the accumulation/depletion layer, is less than 1 micron for a typical 10 Gbps TED design. At this point in time the domain stops growing because the voltage gradient for the (normal) carrier electrons outside the domain has dropped to about half and the corresponding drift velocity for the normal electrons has dropped roughly in half to a value equal to (in equilibrium with) the domain velocity. Total channel current is also roughly halved, independent of subsequent variations in anode voltage or gate voltage.

Summarizing, a small negative going gate voltage triggers a large step decrease in channel current and large step increase in channel resistance. After a predictable time interval the domain reaches the anode and disappears, and the device quickly relaxes back to initial conditions. The overall action is similar to a one shot pulse generator with very high power gain/sensitivity, usable directly as a D flip-flop or a shift register stage since the input data can vary while the triggered domain is present without affecting the output. A negative going output pulse can be taken from the cathode, i.e., developed across a cathode load impedance, or from a midchannel Schottky electrode. A positive going output pulse can be taken from the anode, simultaneously if desired. Multiple trigger-gate electrodes may be deposited on the channel surface to effect OR/AND logic functions in a single TED channel; thousands of such complex logic cells operating at 10 Gbps (each at a few mW dissipation) can theoretically be fabricated on single chip. Equivalent logic-gate delay-power products below 100 femtojoules at 10 Gbps should be attainable for some logic functions within the next few years.

Because the maximum operating rate (corresponding to minimum cycle time or domain transit time) is inversely proportional to channel length, while power dissipation is directly proportional to channel length, TEDs exhibit the unusual property that power decreases with increasing designed operating rate. Thus, TED technology is suggested for bit rates above a few Gbps where power dissipation is relatively low. Extension of operating rates above 10 Gbps requires reduction of TED channel lengths. The associated problems and constraints are discussed later in this section. Circuit time constants at normal operating temperatures also require reduction, primarily by reducing gate lengths below 1 micron.

One promising aspect of implanted monolithic GaAs integrated circuit technology is the possibility of having optimized FET and optimized transferred electron devices (TEDs) on the same chip. For an A/D converter chip, the FET can best provide linear functions, including input S/H and in/out interfacing functions to other chips, while the TED can provide ultra fast decision, logic functions, and timing.

### 3.3.2 Device Design Considerations

TED operating frequency is inversely proportional to the time required for a dipole domain to travel from the point at which it is nucleated to the TED anode where it is collected. Referring to Figure 3-9, the domain transit distance is approximately the distance between the gate and the anode, $\ell_{ga}$, assuming gate triggering of the domains. The domain transit velocity is generally assumed to be equal to the saturated drift velocity of electrons in GaAs, $\approx 10^7$ cm/sec. However, it has been found, after measuring the transit time frequency of a large number of planar TEDs, that the domain velocity varies in proportion to the measured material mobility ($\mu$), and should be so scaled. Therefore, domain transit time is given by

$$T_{transit} = \frac{\ell_{ga}}{1.26 \times 10^7 \text{ cm/sec}} \cdot \frac{8000}{\mu} \text{ at } +25°C \qquad (3\text{-}1)$$

where the maximum theoretical mobility is 8000 $cm^2$/volt-sec, and the saturated drift velocity is $1.26 \times 10^7$ cm/sec.

Two empirical TED design constraints are:

$$n_o \, d \geq 10^{12} \text{ cm}^{-2}$$

$$n_o l_{ca} > 2 \times 10^{12} \text{ cm}^{-2}$$

The device's low field resistance, ignoring depletion under the gate, is given by

$$R = \frac{\ell_{ca}}{nq\mu Wd} \qquad (3\text{-}2)$$

where q = electronic charge = $1.602 \times 10^{-19}$ coulombs.

### 3.3.3 Qualitative TED Design for Gate Controlled Domain Triggering

Consider the device cross-section and field plots of Figure 3-10. If a bias is applied to the device anode with the cathode grounded and the gate floating, the qualitative field distribution is as shown in

Figure 3-10b. Depletion of carriers under the date due to the built-in voltage reduces the effective cross-sectional area there, and causes the higher field under the gate. Now if a gate bias (negative relative to the underlying channel) is added, the channel under the gate will deplete further, causing the field there to exceed the threshold value ($E_c$) and causing a domain to be launched. If the field between the gate and anode is high enough, i.e., above the sustaining level, the domain will propagate down the channel and be collected at the anode. Notice that when the gate bias is increased, the field outside the gate region reduces such that the field integrated over the device length remains equal to the constant applied anode voltage (Figure 3-10c).

If the epilayer is very thin, the depletion depth due to the gate's built-in voltage may be such a large percentage of the channel thickness that it is impossible to bring the field outside the gate up to the sustaining level without exceeding the threshold field under the gate. If this were the case, the device could only be turned on and off by the anode voltage, and the gate would have no control. Another situation, and one that is of particular interest for short (10 Gbps) devices, is that which occurs when the gate occupies a significant portion of the channel length. In this case it might be possible to achieve a field distribution like that of Figure 3-10b for the off state. However, when the gate bias is applied, the field outside the gate region may be lowered below the sustaining level and the domain will not propagate.

To examine these considerations in detail, use is made of Copeland's numerical calculations of the excess domain voltage $V_D$ as a function of E, the field external to the domain. These calculations show that $V_D$ increases from zero (at E equal to the threshold field ($E_c$) to infinity as E is decreased to the minimum sustaining field of about $1.45 \times 10^{-3}$ volt $cm^{-1}$. $V_D$ is a function of concentration as well as applied bias.

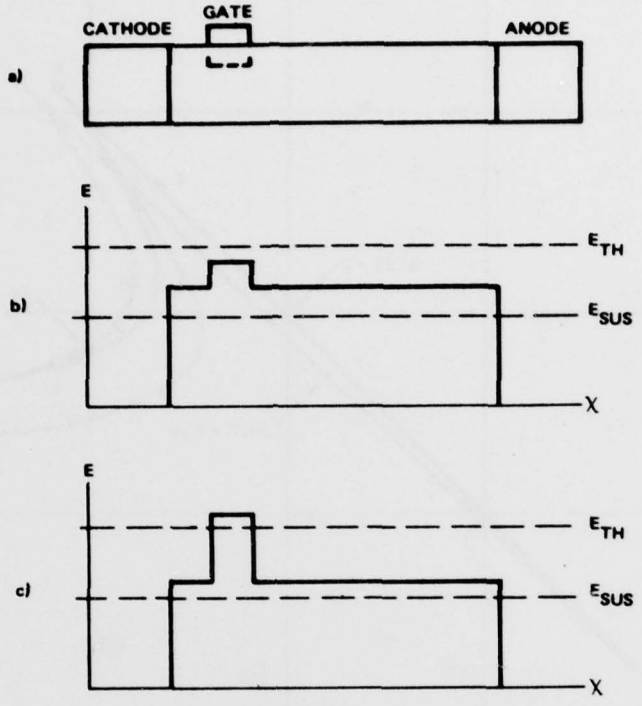



Figure 3-10. Basic Gate Controlled TED and Field Plots Field Plots

Copeland shows that only one domain size is stable in a TED diode with a constant applied anode voltage $V_a$, the anode voltage being the sum of $V_D$ and product $E\ell_{ca}$. Intersection of the straight line representing $V_a = V_D + E\ell_{ca}$ with the curve of $V_D$ versus E gives unique values of $V_D$ and E. A more convenient presentation of this information is shown in curve a Figure 3-11 in which the normalized current versus the applied voltage is plotted for a TED of 10 μm length and $10^{16}$ $cm^{-3}$ concentration. The parameter X on this plot is the fraction of channel depleted by gate bias. The initial, linear portion of this curve is simply the low field ohmic

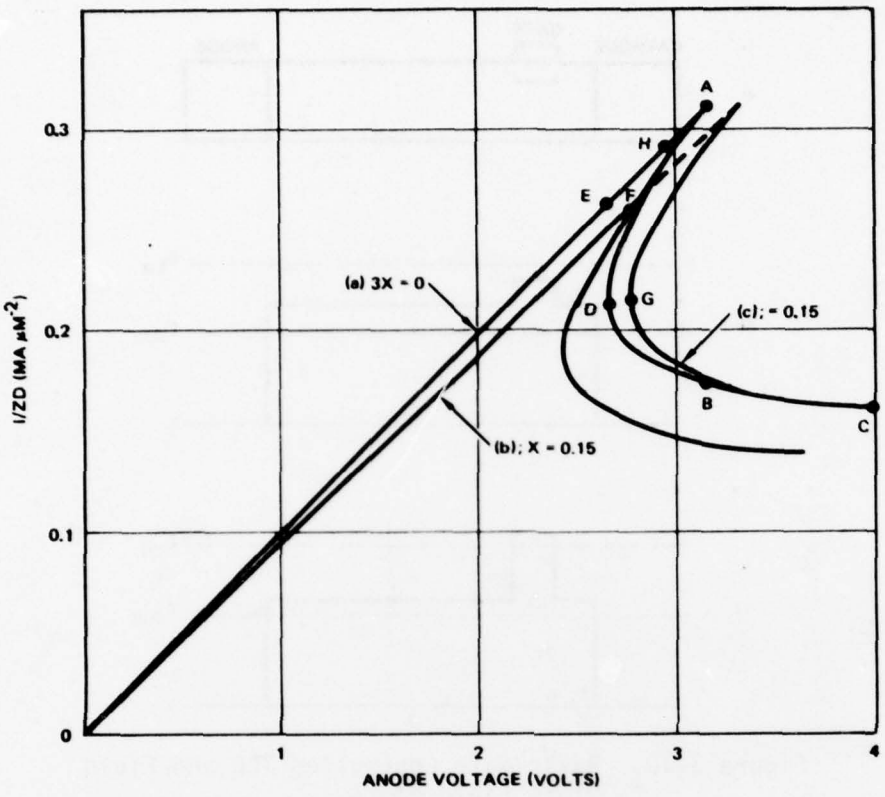



Figure 3-11. Calculated I-V Characteristics of a TED of Length 10 μm $10^{16}$ cm-3. (a) Zero Depletion Region Under Gate. (b) and (c) Fractional Depletion Region, x = 0.15. (b) is Characteristic for Domain Propagating Under Gate While (c) is for the Domain in the Gate-to-Anode Region. Gate Length $l_g$ = 3 μm. Fractional Depletion Depth Divided by Channel Thickness.

behavior of the device when no domain is present. The reentrant and higher voltage portion of the curve is derived from the expressions

$$V_a = V_D + E\ell_{ca} \tag{3-3}$$

and

$$\frac{I}{Wd} = nq\mu E \tag{3-4}$$

where $V_D$ is obtained from the extrapolations of Copeland's results, and 6200 $cm^2$ $volt^{-1}$ $sec^{-1}$ is used for the low field mobility, $\mu$. Use of the low field mobility is valid since E always remains less than the threshold field. These expressions show that the difference between $V_a$ for the reentrant and high field portion of the curve and $V_a$ for the linear potion, for any value of I, is $V_D$.

When the anode voltage is increased from zero, the device is a linear resistor until point A. There a domain is formed and the current drops to point B since a substantial portion of the applied voltage is developed across the domain. If, while the domain is still in transit, the applied voltage is increased, the current follows line BC. With the domain still in transit, if the voltage is reduced below the threshold voltage the current follows BD, but at point D the voltage is insufficient to maintain a stable domain. The domain is quenched and the current rises to point E. The voltage at point D is thus the domain sustaining voltage. Existence of a device characteristic curve of this nature has been demonstrated experimentally by Kurn, Robson, and Kino who have measured the device current as a function of applied voltage while the domain is in transit. Clearly, this curve is not the same as the low frequency I-V characteristic of the device, which is a time average including the period of domain quenching at the anode, and nucleation and growth of a new domain.

Curve b of Figure 3-11 is the calculated characteristics of a TED triode in which the effects of adding a gate of length $\ell_g$ = 3 $\mu$m to the above device is illustrated. For this curve, x = 0.15, where xd is the thickness of the depletion region resulting from the gate bias and x = xd/d. For simplicity, the depletion region thickness is assumed constant under the length of the gate. Curve b illustrates the characteristics while the domain is under the gate and shows that both the current and voltage required to nucleate (point F) and to sustain a domain are reduced since the field under the gate is increased by the presence of the depletion region. When the domain moves into the gate-to-anode region of the device, the field outside the domain is appreciably less than when the domain was under the gate. This is reflected in the fact that if the domain sustaining voltage (the anode voltage required to maintain the domain sustaining voltage (point G) is less than the device threshold voltage (point F), the

domain nucleated under the gate will propagate to the anode. When the domain sustaining voltage is greater than the deivce threshold voltage and the TED is operated at a constant anode voltage between these two values, a domain formed under the gate cannot propagate into the gate to anode region. In fact, considering the domain dimensions are similar to the gate length in this concentration regime, it is possible that a mature propagating domain cannot form. Rather, it appears that a staticnary space charge region forms to satisfy the conditions of negative differential mobility existing under the gate, and the device current becomes independent of anode voltage.

The phenomenon exists in the current saturation region of GaAs FETs in which the short device length and appreciable value of x result in a domain-sustaining voltage substantially in excess of the threshold or saturation voltage. This also explains the current saturation observed in some TED structures at a lower anode voltage than that required to nucleate domains. It appears that in these cases, propagating domains cannot be formed unless the anode voltage exceeds at least the domain sustaining voltage.

Current dropback upon domain formaton can also be estimated from curves of the type shown in Figure 3-11. For example, suppose the device is held in its quiescent state with x = 0 at the point H on curve a, just below the threshold voltage on this curve. If the device is held at a constant anode voltage, a domain will form and propagate when a gate voltage sufficient to cause a depletion region of x = 0.15 is applied, since the anode voltage is above both the threshold voltage and sustaining voltage. The current during domain propagation is given by the curve at that anode voltage. The effect of a load resistance can also be determined by employing the conventional load line construction on this curve.

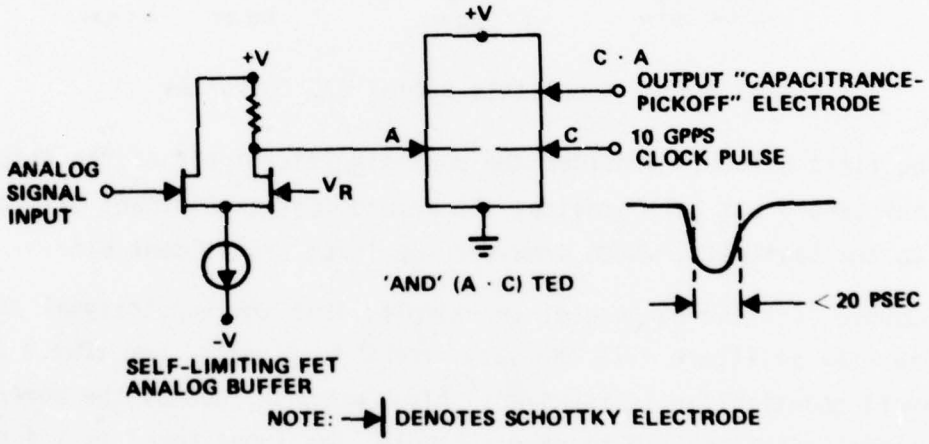
Recent detailed analysis have shown that the aforementioned problem of insufficient sustaining voltage in short (e.g., 10 Gbps) TEDs is readily overcome by the following techniques:

- Reduction of gate length, $\ell_g$ to roughly one micron

- Increase in net donor concentration, $n_o$ (for example, to roughly $3 \times 10^{-6}$ $cm^{-3}$)
- Minimization of gate depletion into the channel, e.g., by selective impurity implantation.

### 3.3.4 Gate Controlled TED Threshold Comparator

From the foregoing considerations the characteristics listed in Figure 3-12 are estimated to be attainable within the next few years for a 10 Gsps threshold comparator. The FET stage must prevent both excessive forward current and excessive reverse voltage to the TED input electrode A while isolating (buffering) the analog input line from the TED triggering kickback. The TED triggers only when both A and C inputs are sufficiently negative (causing the field underneath to approach 3.2 kV/cm).




APERTURE WINDOW < 20 PSEC
ANALOG BANDWIDTH > 4 GHZ
EQUIVALENT ANALOG INPUT UNCERTAINTY < 30 MV

$P_{DISS}$ < 20 MW (EXCLUDING POWER FOR CLOCK GENERATION)
CLOCK-TO-OUTPUT DELAY = 40 PSEC TYPICAL
OUTPUT RISETIME < 25 PSEC

Figure 3-12. TED/FET Threshold Comparator

### 3.3.5 TED/FET A/D Converter Configurations

#### 3.3.5.1 Serial TED/FET A/D Configuration

An organization which takes advantage of TED properties is the serial organization. This organization (Figure 3-13) is very efficient in terms of the number of devices and dc power consumption. However, it does require close tolerances in the circuit fabrication.

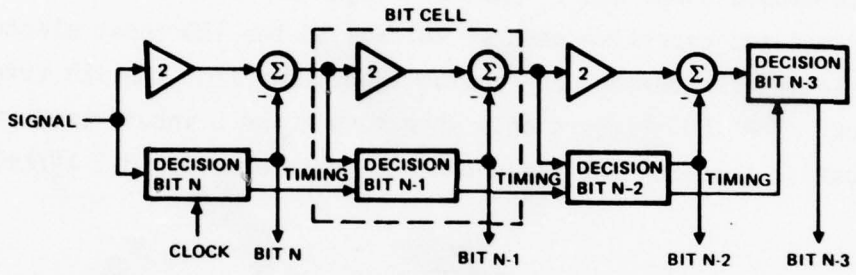



Figure 3-13. Monolithic Serial A/D Converter

The first bit cell provides the most significant bit of the output word, the second bit cell provides the second most significant bit, and so on to the last cell, which provides the least significant bit.

Suppose, for the purpose of an example, that the input signal to the A/D converter of Figure 3-13 can vary from 0 to 4 volts, and that 4 bit (16 level) quantization is required. Also, suppose that at the moment the clock signal tells the A/D to take a sample, the input level is 1.4 volts, requiring a digital representation "0101". The decision bit N circuit examines the input to determine whether or not it exceeds 2 volts. Since it does not, the decision circuit provides no output pulse, that is, a digital "0"; and the linear amplifier doubles the amplitude and provides the doubled amplitude to the summer. The other summer input is the decision bit output, either 0 or -4 volts. The summer takes the difference of 0 volt and 2.8 volts (2 x 1.4 volts) and feeds the 2.8 volts forward to the next bit cell. The next cell again determines whether or not its input exceeds 2 volts. Since it does, the decision circuit provides an output pulse, and the difference circuit subtracts 4 volts from the 5.6 volt amplifier input to the summer, leaving a 1.60 volt input to the next

cell. The third bit cell provides a "0" output since its input is less than 2 volts, and feeds forward 3.2 volts to the final cell. The input to that cell exceeds 2 volts, and so its output is a "1". Thus, the required "0101" output code has been provided.

Operation of each individual cell (Figure 3-14) may be compared to the block diagram of the basic cell shown in Figure 3-12. The input to the A/D cell is fed into one side of a differential FET pair which serves as the amplifier in the cell. The left FET $F_A$ amplifies the incoming signal and feeds it into the TED $T_B$, which is the decision element of the cell. The decision element $T_B$ is clocked by the output of TED $T_A$. When the input to the cell is in the upper half of its range, $T_B$ is triggered, generating a "1" at the bit output. The right FET $F_B$ sums the amplified input and the bit output which are fed forward into the next cell. The lowest aperture time would be obtained by incorporating an on-chip FET S/H circuit at the A/D input. The following characteristics are estimated for a single chip monolithic 4 bit 10 Gsps serial quantizer, in a regulated-temperature environment:

- Analog input-to-digital (throughput) delay <500 psec
- Analog input range: ±1.6 V into 50Ω
- Analog bandwidth >4 GHz
- $P_{diss}$ = 1 watt

The restriction of a regulated temperature environment is brought about by a current lack of information or test results on the temperature dependance of GaAs TED parameters.

3.3.5.2 Parallel TED/FET A/D Configuration

A parallel A/D quantizer is illustrated in Figure 3-15. The FET S/H would be used to minimize aperture effects when required. The FET amplifier provides an increased-amplitude linear analog signal to $2^N$-1 FET/TED threshold comparators previously described in Section 3.3.4. Setting the comparator input uncertainty $\Delta V$ (less than 30 mV) equal to 0.3 LSB, the required FET amplifier output swing.

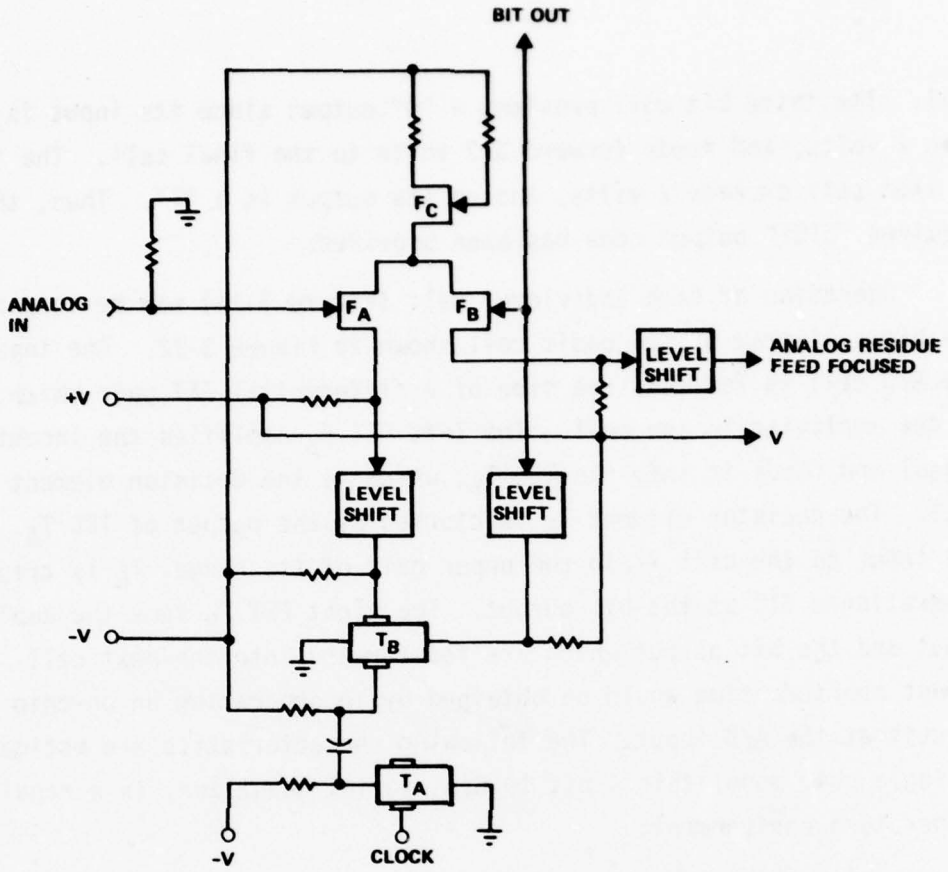



Figure 3-14. Single Cell of Serial A/D Converter

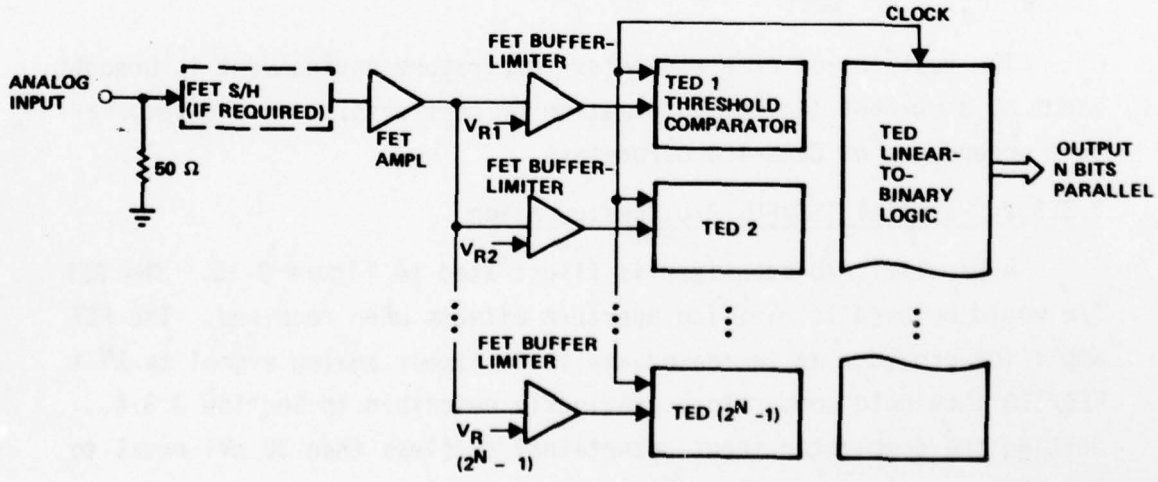



Figure 3-15. Parallel TED/FET A/D Quantizer

$$V_{p/p} \simeq \frac{2^N \Delta V}{0.3}$$

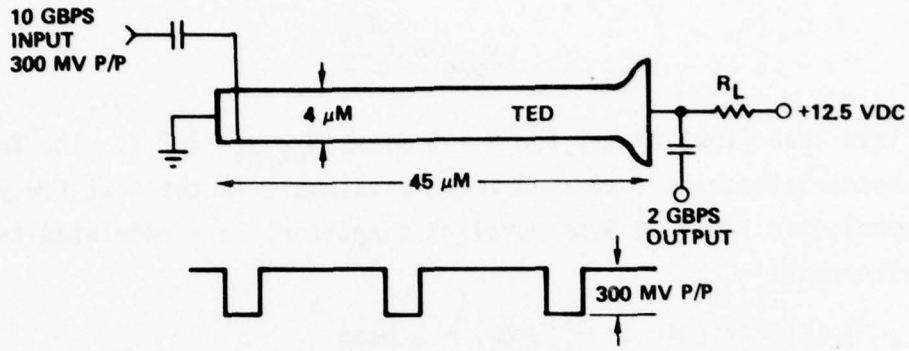
is less than (100) $2^N$ mV; for N = 5 bits, $V_{pk/pk}$ <3.2 V. The following characteristics are estimated to be attainable in the next few years for a monolithic 5 bit 10 Gsps parallel quantizer, in a regulated-temperature environment:

- TED trigger time ($\equiv t_T$) $\simeq$ 5 psec
- Clock generator pulsewidth ($\equiv PW_0$) <20 psec
- A/D aperture time window $\doteq \left[(PW_0)^2 + (t_T)^2\right]^{1/2}$ <20 psec
- Analog input-to-digital output (throughput) delay <350 psec
- Analog input range: $\pm$1.6V into 50 $\Omega$
- Analog bandwidth: >4 GHz
- $P_{diss}$: = 1.8 watts

### 3.3.6 Associated TED Digital Functions

TEDs are monostable two-state (domain or no domain) devices that are directly suited for binary logic functions, expecially at > 5 Gbps rates (for low power consumption). The inherent triggering and short term storage properties, along with use of additional control electrodes, result in complex logic capability at very low device count and small chip area.

Frequency divider (timing generator) functions and narrowband shift register functions are especially simple to implement. The "TED plus $R_L$" total device area for the example frequency divider of Figure 3-16 is about 4 microns x 50 microns. The only other devices are input and output coupling capacitors which can be incorporated into the signal (interconnect) lines by forming a small 4 x 4 $\mu$m dielectric sandwiched between two interconnect-metal layers. The basic principle of operation is that once the input triggers a domain the low-frequency output is insensitive to the applied high-frequency input for almost the entire output duty cycle until the domain disappears at the anode.




ACTIVE LOW-FIELD CHANNEL RESISTIVITY = 1000Ω/□

$$\text{AVG} = \frac{0.2\ \text{V}/\mu\text{M}}{1000\Omega/\square \times 1/4\ \square/\mu\text{M}} = 0.8\ \text{MA FOR Z} = 4\ \mu\text{M}$$

$P_{DISS}$ = 12.5 V (0.8 MA) = 10.0 MW

Figure 3-16. ÷5 Narrowband TED Frequency Divider

Figure 3-17 illustrates a low device count 10 Gbps 8:1 demultiplexer utilizing TEDs having a "capacitive pickoff" Schottky output electrode, located on the channel surface midway between cathode and anode. The smaller TEDs (4 x 10 μm each) form a serial 10 Gbps shift register, and the larger (10 x 10 μm each) TEDs are simple AND gates (both the opposed trigger electrodes must swing roughly 300 mV negatively to trigger a domain) which AND the 1.25 Gbps readout clock with the shift register output digital data to provide eight simultaneous parallel pulsed data outputs.

### 3.3.7 TED Potential for Future Navy Systems

Projections for TED/FET digital technology are relatively tentative because the technology is presently in a very early stage of development. In contrast to GaAs FET technology, a chip having the equivalent logic power of an MSI function has not yet been developed. Such a chip development is expected within roughly 2 years but the rate and direction of development in general depends heavily on government interest or demand. Second, the direction of development may shift with technological breakthroughs in the near future. Relatively unexplored areas of TED digital technology include transverse-domain-propagation logic, majority logic, and bistable TED logic. Bistable logic is expected to involve trapping/untrapping of a domain within the TED (near the anode).

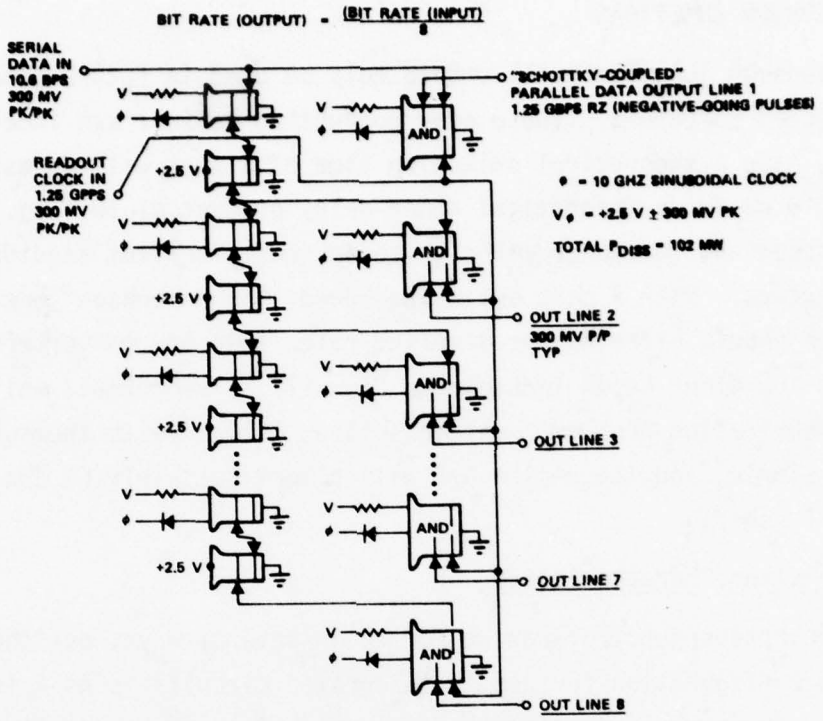



Figure 3-17. 8:1 TED Demultiplexer

In general, TED clock and/or data input rates of roughly 5 or more GHz are suggested for low power dissipation.

Applications requiring the least technology development would include frequency dividers and shift register functions.

A listing of digital applications (for a single GaAs chip) in increasing order of development time would be as follows:

- Narrowband frequency dividers
- Narrowband frequency dividers with instantly commandable division rate
- Digital multiplexers and demultiplexers
- Digital correlators
- Encryptors
- General data storage registers or devices
- Digital pipeland multipliers and arithmetic processors
- A/D converters as described in Section 3.3.5.

## 3.4 JOSEPHSON JUNCTIONS

Josephson junctions will undoubtedly be used in future generations of high speed computers. These superconducting devices are inherently bistable, have a theoretical switching time of 1 psec with an associated power of 10 nW for a theoretical power-delay product of $10^{-8}$ pj. This extreme speed and low power makes these devices excellent candidates for A/D converters. With a psec switching speed, the Josephson junction A/D converters should offer higher sampling rates than A/D converters implemented in any other known technology. It will be seen that, while some serious fabrication problems must be solved, the circuits themselves should be quite simple, and the entire A/D will almost certainly be contained on a single IC chip.

### 3.4.1 Junction Characteristics

A Josephson junction can be formed in several ways, but the most promising configuration for use in integrated circuits is as a tunnel junction. The tunnel junction is formed from two superconducting materials separated by a thin insulating barrier. When the junction is cooled below its critical temperature, the materials become superconducting and electrons can tunnel through the insulating barriers. For currents less than some critical value, the barrier provides no resistance to electron flow and no voltage drop is developed across the junction. In this case the junction is said to be in the superconducting or current state. When the junction current exceeds the critical current, the junction goes "normal" and has a finite resistance. The junction is then said to be in its voltage state because a voltage appears across the junction. If the junction is in parallel with an appropriate resistance, the voltage developed across the junction is a constant value referred to as the gap voltage.

The current and voltage states of the junction are utilized to perform binary logic functions. A magnetic field applied to the junction decreases the critical current and allows one to switch the junction from its current to its voltage state. The switching fields can be provided by current-carrying wires routed near the junction. Because switching is determined by both the current through the junction and the total magnetic flux in the barrier region, Josephson junctions provide unique opportunities for logic circuit design.

Tunnel junctions are readily adaptable to planar geometrics and thus to large scale integration techniques. Present research efforts are directed toward optimizing logic circuit designs and junction fabrication processes. The efforts have already produced experimental chips incorporating thousands of junctions.[1] Development of Josephson junction logic circuits and memories will provide the support for A/D converters and much of the expertise needed for converter design and fabrication.

The power-delay products for Josephson junctions are the smallest known. A switching time of 34 psec at 0.1 μW has been reported[2] for a power-delay product of $3 \times 10^{-18}$ j. Both switching speed and power dissipation can be improved by at least an order of magnitude. However, for the near future these figures probably indicate the level of performance that can be expected from Josephson junction integrated circuits.

### 3.4.2 A/D Converter Design

The design of Josephson junction A/D converters could be based on several different junction configurations. The various schemes can be divided into two groups:

1) Digitize/encode includes schemes in which the amplitude of the analog signal is initially digitized by a circuit. The digital representation is then converted through the use of logic circuits to the proper binary code.

2) Direct encoding is made up of circuits in which junctions are combined to produce a binary code directly.

#### 3.4.2.1 Digitize/Encode Conversion Schemes

Any scheme using ramp conversion would fall into the first group. Josephson junctions can be arranged to generate a stepped ramp function which can be compared to the analog signal. The output is sent to a binary encoder. The accuracy of such a scheme depends upon the precision with which the steps can be generated. A Josephson junction ramp generator can be based on the gap voltage of the junctions. The gap voltage is determined by the superconducting material and is only dependent on temperature. For niobium, a common junction material, the gap voltage varies by 3%/°K at 4.2°K. However, the temperature of a liquid helium bath is easily regulated to within a millidegree. The gap voltage is then constant to better than 0.005 percent. In principle, the gap voltage could thus provide a ramp for a 12 bit A/D converter.

A second conversion scheme, similar to ramp conversion, utilizes a superconducting loop. When one or more Josephson junctions are included in a closed loop, quantum interference occurs. The magnetic flux enclosed by the loop is quantized and any change occurs in discrete amounts. With an analog signal applied to the loop the flux jumps can be counted by the appropriate ancillary circuitry and converted to binary code.

Both of these methods are inherently quite accurate because they are based on a very stable step size. However, the need to generate a ramp makes the device slow by comparison to a more direct method of conversion. In addition, the circuits would be much more complex due to the required logic functions. To realize the high speed possible with Josephson junctions it is necessary to design a more direct form of conversion.

3.4.2.2 Direct Encoding Conversion Schemes

As an introduction to direct conversion schemes, an A/D converter design proposed by Fang and Herrell[3] will be considered in detail. It illustrates many of the features of Josephson functions. The circuit required for a 3 bit converter is shown in Figure 3-18. Analog signal $V_{IN}$ is applied across three sets of Josephson junctions, $J_1$-$J_7$, and resistor $R_{IN}$ all connected in series. Initially, all the junctions are in their current state and are superconducting. Thus, $V_{IN}$ drives a current limited by $R_{IN}$ through the junctions.

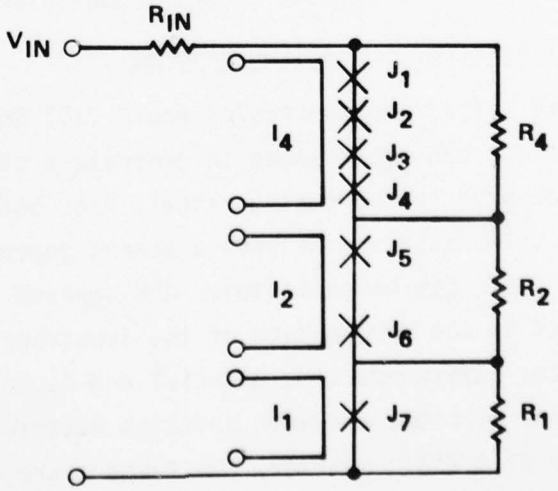



Figure 3-18. A/D Converter Using Josephson Junctions as Proposed by Fang and Herrell

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HIGH SPEED A/D CONVERTERS SYSTEMS APPLICATIONS STUDY.(U)
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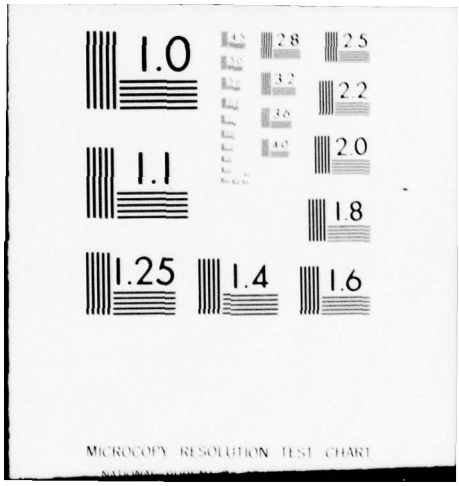
1.0
1.1
1.25
1.4
1.6
2.8
3.2
3.6
4.0
2.5
2.2
2.0
1.8
MICROCOPY RESOLUTION TEST CHART

The circuit outputs are developed across the resistors $R_4$, $R_2$, and $R_1$ which are connected in parallel with 4, 2, and 1 junction, respectively. The output is 0 if no voltage appears across the resistor and 1 when a voltage does appear. With the juctions in their current states, the outputs are 0's. However, when the current through any set of junctions exceeds their critical current level, that set switches to the voltage state. The voltage developed across each junction in the set is gap voltage $V_g$ if the value of the corresponding parallel resistor is appropriately chosen.

As an example, if the critical current of junctions $J_1$-$J_4$ is exceeded, a voltage of $4V_g$ will develop across the junctions and $R_4$. Notice that $V_{IN}$ would then be decreased by $4V_g$ and the current flowing through the circuit would be reduced. However, junctions once switched to their voltage state remain in that state until the current drops below a threshold for latching which is less than the critical current.

The critical current for each of the three sets of junctions is determined by the bias currents $I_4$, $I_2$, and $I_1$. Specifically, $I_4$ produces a magnetic field through junctions $J_1$-$J_4$ that depresses their critical current. Likewise, $I_2$ controls $J_5$ and $J_6$ and $I_1$ controls $J_7$. The control biases are adjusted such that $J_1$-$J_4$ switch when four units of current flow through them, $J_5$ and $J_6$ switch when the current reaches two units, and $J_7$ when 1 unit of current flows.

In operation the analog signal is applied with all junctions in their current state. Then $I_4$, $I_2$, and $I_1$ are applied in that sequence. If the current due to the analog signal is greater than or equal to four units, $J_1$-$J_4$ will switch when $I_4$ is applied and a 1 is read across $R_4$. However, the voltage developed across $J_1$-$J_4$ then reduces the current by four units. When $I_2$ is applied, $J_5$-$J_6$ switch only if the remaining current is greater than or equal to two units. If its is, a 1 is read out as the second MSB and the current is reduced by two units. Finally, $I_1$ is applied to determine if one unit of current remains. In this way, the analog input is directly converted to a binary output.

The circuit operates within two constraints. First, the maximum input signal cannot cause the current to exceed the critical current of an unbiased junction. Thus, $2^N$ units of current, where N is the number of bits, must be less than the unbiased critical current. Second, one unit of current, which corresponds to the LSB, must be greater than the latching threshold of the junctions. These constraints, particularly that due to the latching threshold, limit the number of bits that can be produced.

Other converter designs which provide a binary encoded output directly usually incorporate two functions: S/H function and a feedback or correction function. In the first section the analog input is used to trigger parallel stages as its amplitude surpasses 1, 2, 4...N times the LSB size. The accuracy of this S/H function is determined by the uniformity of the junctions. Junction uniformity, measured in terms of critical current, is determined by the physical dimensions of the barrier and the junction composition. Present fabrication techniques can produce current matching to about 10 percent. Such matching is sufficient for development of a 4 bit A/D converter.

Nonuniformity in junction fabrication can be corrected by providing an adjustable bias field for each junction. The accuracy of the resulting circuit is then dependent on the precision with which the bias can be set and maintained.

The second section of most direct A/D converter schemes provides a feedback or subtraction function which can produce zeros when required for the LSBs. The requirements for junction uniformity can be much more stringent in this section. The accumulated error is $2^N$ times the difference in junction critical currents.

Accuracy in the subtraction section can be substantially improved by basing the feedback on the gap voltage rather than the critical current. An experimental A/D chip has been fabricated by IBM[4] which uses Josephson junctions. The converter has a 4 bit output and uses the direct conversion method. The first section uses field biased junctions while the second section depends upon the gap voltage of junctions to provide the subtraction function. The chip has operated at up to 62.5 Msps.

The sampling rate of the IBM chip[4] was limited by the external signal generators used to operate the circuit. It is believed that Josephson junctions can be switched in as small a time as 1 psec. Therefore, a circuit speed will be mainly determined by the propagation delay times in the circuit and the associated functions. Because a Josephson junction A/D converter requires various sampling and control pulses, it is necessary to design signal generators which can match the inherent speed of the converter itself. A reasonable source of such functions is a pulse circuit also designed using Josephson junctions. Thus, any converter design should also include the triggering and pulse producing elements.

### 3.4.3 Cryogenic Consideration

Any consideration of Josephson junction devices must also include the cooling system. Although liquid helium temperatures are routinely maintained in laboratory environments, efficient, self-contained methods for providing long term cooling to 4.2°K remain to be developed. Laboratory cooling is usually obtained by immersing the object to be cooled in a bath of liquid helium. The bath is contained in a vacuum insulated vessel or dewar. The helium that boils away is either replenished from a larger storage dewar or through the use of commercially available recirculating helium liquifiers.

Because Josephson junction circuits dissipate such a small amount of power, circuits could be partially sealed in dewars containing enough liquid helium to last for the lifetime of the circuit. The capacity of such a dewar would be primarily determined by the heat loss through the walls of the dewar and the electrical connections to the circuit in the bath. Designing a dewar with a lifetime of around five years should be possible using present technology if the dewar is used in a vibration free environment.

The cryogenic temperatures required for Josephson junction A/D converters will make their use necessarily more expensive than other room temperature technologies. To justify the added cost and complexity, it will be necessary to incorporate additional superconducting circuitry. As previously noted, to retain the speed of a Josephson junction A/D converter, it will be necessary to also use junctions for the production of

control pulses. To justify the system cost; converter, control, and other signal processing circuits must be integrated using superconducting technology whenever possible.

### 3.4.4 General Considerations

Other factors to be considered in evaluating Josephson junctions for A/D converters include size, weight, and reliability. Because the circuits can be integrated on a chip, the size and weight of the system are determined by the surrounding dewar or other cooling apparatus. Calculations made at TRW indicate that a cryostat for space applications could have a volume of less than 1000 $cm^3$ and provide a circuit lifetime of 5 years. Such a dewar would weigh on the order of 1/2 Kg when filled with cryogenic liquids.

The system reliability would be largely determined by the cooling system. For space applications a pressure regulated dewar would be required. Ground based systems could be dependent on periodic replacement of cryogenic fluids. Josephson junctions have in the past been very susceptible to damage. Many types of junctions deteriorate after repeated thermal cycling or after storage at room temperature. Current efforts are under way to improve junction resistance to thermal cycling and room temperatures by optimizing fabrication techniques and material choice. Considerable progress has been made in this direction. Junctions are also susceptible to damage by excessive current pulses and, of course, circuit operation would be impaired by exposure to external magnetic fields. Therefore, suitable circuit protection would have to be included in the system design.

### 3.4.5 Future Potential

The additional complexity required to cool Josephson junction circuits will limit their use as A/D converters to applications in which other superconducting circuitry is being used or applications in which the higher sampling speed is necessary. Development of very small junctions with psec switching times will allow the design of direct conversion circuits with cycle times of tens of picoseconds. The resulting A/D converters should be capable of sampling speeds of perhaps 50 Gsps. In addition to high speed,

the converters will also reduce power dissipation to submicrowatt levels. While desirable, low power dissipation alone will not justify the use of Josephson junctions.

The accuracy of future Josephson junction A/D converters is harder to predict. In principle, even direct conversion should be possible with high accuracy. However, accuracy depends on precision fabrication of junctions and the associated magnetic bias, control, and feedback lines. Presently, 4 or 5 bit accuracy is possible. Additional accuracy can be expected with improved resolution during fabrication and careful design of magnetic biasing for individual junctions. Alternatively, it may be possible that by using a hybrid of circuit designs, more of the A/D conversion can be accomplished using only the gap voltage of the junctions. For example, the Fang and Herrell scheme described above could be used to produce the MSBs and a precisely reduced signal to be converted using some other circuit. Such a scheme would immediately improve accuracy. Using one of the methods described here or some hybrid scheme, it is reasonable to expect future A/D converters operating at high speed with 8 bit accuracy.

To develop such converters, research into several areas will be required. Development of junction fabrication techniques must be continued to produce increased uniformity and resistance to aging effects. Increased resolution in all circuit component layouts is also desirable. Of course, the actual design of the A/D converter circuit must be addressed, but in addition, there is also the need for control pulse circuits. Mechanical design of an appropriate cooling system is required and must be developed. Finally, integration of the circuit into a total signal processing system must be investigated as a means of justifying the use of Josephson junctions.

## 3.5 ELECTRO-OPTIC

Two types of A/D conversion technologies fall under the heading electro-optic (EO). The first modulates and/or deflects an electron beam with an analog signal. Time samples of this signal can be taken by either gating the electron beam with short pulses or by continuously deflecting the beam past fixed targets. The electron packets can be deflected by the analog signal to hit an area of the target that is associated with the corresponding analog amplitude and encoding done separately. The continuous swept electron beam can be deflected perpendicular to its time sweep path for direct amplitude encoding. Electron beam semiconductor (EBS) devices have been applied to implement EO A/D converters. The target in an EBS A/D conversion tube is comprised of an array of semiconductor diodes that normally do not conduct. When the electron beam or packet hits the diode, the electrons create carriers in the junction and thereby identify where the electron packet was deflected. Direct coding of the digital data can be achieved by deflecting a sheet beam of electrons and arranging the detector diodes to produce any desired code. A Gray code is most appropriate to reduce the magnitude of any error that may occur from the electron beam being deflected between adjacent junctions.

The potential for EBS approaches to A/D conversion have been estimated by Watkins-Johnson, the principal proponent of this approach, as 6 to 10 bits resolution and sampling rates up to 1 or 2 GHz. The principal deficiencies of the EBS approach arise from its reliance on an electron tube. Watkins-Johnson has worked on EBS A/D converters under sponsorship of the U.S. Army Ballistics Missile Defense Advanced Technology Center (BMDATC). This development was an attempt to use EBS techniques to perform 250 MHz, 8 bit conversion. The major components of the device were a sheet beam electron gun, beam chopping structure to provide a narrow aperture, analog deflection structure to be controlled by the analog input, and semiconductor target which was to produce the 8 bit output code. The electron gun development did not result in a device that would meet specifications.

Another Watkins-Johnson development of an EBS A/D is being funded by the U.S. Air Force Rome Air Development Center. Rather than using a sheet beam gun, this development employs a conventional single beam electron gun that is deflected in a circular pattern by the analog deflection structure

where the radius of the circle is proportional to the analog input signal amplitude. The semiconductor target disk has a mosaic of $2^N$ annular rings that are separated into wedge-shaped sectors. As the electron beam transverses each sector, one conversion of the input signal is performed to an N bit word with a value corresponding to the annular ring struck by the electron beam. The development effort is an attempt to build a 6 bit, 10 sector device with a beam revolution rate of 200 MHz, thereby giving an effective sampling rate of 2 GHz.

The second EO A/D conversion technology utilizes a laser beam instead of an electron beam. A variety of ways to operate on a laser beam include: deflection, polorization rotation, intensity modulation, and phase retardation. The Naval Ocean Systems Center, San Diego, California is developing an EO A/D which has the potential for 6 to 8 bit resolution and conversion rates approaching 1 GHz. The A/D makes use of the fact that the output from an optical intensity modulator, the operation of which is based on a linear EO phase retardation, varies in a periodic fashion as a function of the applied voltage. Optical intensity modulators consist of a waveguide structure etched on a substrate (e.g., lithium niobate) and electrodes which are used to retard the phase in one waveguide relative to the phase in another, as a function of the applied voltage. For a 6 bit EO ADC, it is expected that the length of the required substrate is approximately 1.7 cm.

In terms of overall power dissipation, the optical device offers an improvement over conventional A/D converters, primarily because of the reduction in power required for comparators. The comparator function in the EO converter requires only 3 watts. Assuming 0.3 watt for a laser source, 0.4 watt for the EO portion of the device, and 0.3 watt for each of the 12 photodetector/amplifiers the total EO A/D converter power is estimated at 7.3 watts.

## 3.6 SOLID STATE FABRICATION TECHNOLOGY

This section is concerned with the common denominator of all technology work, namely the fabrication techniques and limitations. Section 3.6.1 considers E-beam lithography. Both the near-term and the longer term advantages are described. Section 3.6.2 evaluates the limitations in bipolar and MOS devices, resulting in estimates of minimum gate sizes. This is extended in Section 3.6.3 to estimate the ultimate size limitations.

### 3.6.1 Mask Fabrication with E-Beam Lithography

The current state-of-the-art of LSI fabrication and processing is based upon photolithographic processes in which photographic (glass) masks are placed in sequence in close proximity of 3 inch wafers, and then exposed to an ultraviolet light source to form a pattern in an applied photoresist coating over the surface of each wafer. Some LSI manufacturers are still using contact printing to achieve good line definition, though the trend is definitely moving toward proximity and projection equipment for wafer photoresist exposure.

At present, only Canon and Perkin-Elmer are building and marketing projection alignment equipment. Other US equipment companies such as GCA and Cobilt are currently investing millions of dollars to capture this growing market; the driving force is increasing competition among LSI manufacturers to produce faster devices and higher density on 3 and 4 inch wafers.

The majority of LSI manufacturers are using negative photoresists which permit faster processing than available positive resists. The areas of the photoresist that have been exposed to the ultra-violet light source are made either soluble or insoluble to the PR developer, depending upon the type of photoresist selected.

The practical limits of circuit element size are controlled by the optical resolution of the aligner's lenses; these limits are also dependent upon mask-to-mask registration errors which play an important role in a 6 to 12 mask operation as generally required for LSI fabrication. These primary limitations are further compounded by irregularities in wafer flatness and sub-microscopic variations in the wafer's surface due to polishing operations. Other circuit element size limitations are the result of diffraction properties of the aligner's lenses; current limitations on the

resolution of optical (projection) aligner's is about 0.7 microns for 2-1/4 inch wafers; the depth of focus of current projection lenses are not capable of handling flatness variations resulting from the processing of 3 and 4 inch wafers; here, line widths are limited to approximately 4 to 5 microns.

Electron beam lithographic techniques are considered by many as the worthy successor of current optical projection technology. A significant number of companies have made multi-million dollar investments in designing and producing E-beam exposure systems for the forthcoming world-wide market. E-beam lithography is touted by many as the ultimate approach to high density LSI circuits and sub-micron geometries. There are many technical problems that must be resolved before E-beam lithography is adopted by the majority of LSI manufacturers.

In E-beam lithography, the desired pattern in an electron-sensitive photo-resist is formed by scanning an electron beam that is driven by beam-deflection circuitry from a stored program pattern generator; the stored program is used to drive the deflection coils or electrodes of the E-beam machine, putting the programmed pattern onto a chrome-glass mask, or perhaps directly onto a wafer. Initially, E-beam machines will be used to create masks rather than expose electron-sensitive photoresist applied directly to the surface of wafers. Masks patterned by E-beam lithography will contain higher density patterns and generally one to two micron geometries (a significant improvement over the more conventional laser-driven optical pattern generators, now capable of 2 to 3 micron geometries).

The ability to use E-beam lithographic equipment for direct patterning of wafers must await the implementation of E-beam equipment that scans and exposes significantly faster than currently available machines.

Fundamentally, E-beam equipment has greater resolution and depth of focus than optical pattern generators and aligners. It is therefore possible to produce circuits with smaller gate structures and higher levels of circuits integration. Conventional methods of fabricating optical chrome-glass masks limits ultimate optical resolution and mask-to-mask registration accuracy; this impacts on overall yield. E-beam pattern generators will make a significant difference by permitting increased density with no corresponding loss of yield. An E-beam pattern generator

would initially implement chrome master mask fabrication which would improve line-width control as well as line edge quality. Mask defect density will still be dependent upon glass surface quality, methods of applying the chromium films, uniform application of the electron-sensitive photoresist film, photoresist film sensitivity, methods of PR film removal, etc.

E-beam exposure of electron-sensitive photoresist must be accomplished in a vacuum; this necessitates a significant increase in machine complexity to ensure accurate ($\pm$ 500Å) repeatable mask registration inside the machine's vacuum chamber. Visual verification of each mask's position before patterning is impractical due to the complexity of optics involved in assuring appropriate magnification of various registration marks. This critical problem,becomes the key forcing function in designing automatic alignment equipment which will operate in a satisfactory manner inside an ultra-high vacuum system. Automatic alignment may depend upon the use of secondary electron emission from special indexing structures processed into each mask's surface during normal mask fabrication. (The use of these special indexing structures providing secondary emission are already used by some LSI companies that are directly patterning onto wafers rather than using E-beam equipment for master mask processing.)

The sequential patterning of masks (or wafers) using E-beam deflection is basically a SLOW process; attempts to increase scanning speed by employing higher beam currents degrades line resolution due to space charge beam spreading.

The premise implicit in E-beam lithography can be summarized as follows:

- Short term advantages includer higher yields and increased densities by providing E-beam generated glass or quartz master masks that are superior to those obtainable from optical pattern generators
- Longer term advantages include lower cost, better yields, higher densities by direct wafer exposure methods that eliminate masks entirely from the lithographic process
- Specifically, the reduction of device geometries will enable a larger number of LSI chips per wafer, with a corresponding decrease in unit cost/yield factors. Reduced geometries will also enable an increase in circuit operating speed

- Alternative techniques to beam scanning that offer all of the high resolution potential inherent in E-beam lithography (line definition $\leq$ 0.5 micron) may be forthcoming while providing instant overall exposure of the electron-sensitive photoresist much like currently available optical projection systems.

### 3.6.2 Factors Affecting the Size of LSI Circuits

In-depth knowledge of current photolithographic processes and E-beam lithography enables an accurate prediction of the size limitations associated with MOS, CCD and bipolar technologies. B. Hoeneisen and C.A. Mead have explored the limitations applied to planar devices; they believe the key limiting factor is the thickness of the carrier-free depletion zones in PN junctions which cannot be reduced beyond the onset of avalanche breakdown in the device; this is primarily due to the very large electric fields existing in such zones. Keyes (Reference 5) has developed an empirical formula for the breakdown field, $E_B$, in silicon vs doping density N:

$$E_B = 5.6N^{0.3} \text{ volts/cm} \qquad (3\text{-}1)$$

N = number of doping impurity atoms/$cm^3$

Another important relationship is that expressing the depletion zone width of an abrupt PN junction between one lightly doped region and a heavily doped region of silicon:

$$\omega = 2E_{si}\,(V + V_G)N_q \qquad (3\text{-}2)$$

$V_G$ = Forbidden bandwidth (in volts)
$\omega$ = depletion width (in cm)
$E_{si}$ = dielectric constant, Si ($10^{-12}$ farad/cm)
N = Impurity concentration (atoms/$cm^3$)
q = Electronic charge ($1.6 \times 10^{-19}$ coulomb)
V = Sum of chemical potential difference and applied voltage

The electrodes of a bipolar transistor are isolated from each other and from the substrate by PN junctions. These junctions can be reduced to some finite limit where the electric fields would exceed avalanche breakdown limits. The potential difference across a PN junction is equal to the sum of the externally applied voltage and the internal electron chemical potential difference between N and P type silicon. A collector junction is usually operated with an applied potential which adds to the internal potential difference, while an emitter has an applied potential opposite to, and usually less than the internal potential difference.

The area of a planar bipolar transistor is comprised of conducting regions or electrodes separated by PN junctions. The electric field is not permitted to exceed the maximum permissible value $E_B$, at which point breakdown of the silicon's crystal structure occurs. Each PN junction is assumed to be planar, with an abrupt transition from a heavily doped region a more lightly doped background material having uniform distribution of the background dopant. The electric field of such a junction is greatest adjacent to the heavily doped region, vanishing in the conducting region of lightly doped material. The electric field varies linearity in between the heavily doped region and the conducting region. This can be expressed by:

$$E_x = \frac{N}{E_{Si}} X, \tag{3-3}$$

where

$N$ = Impurity concentration

$E_{Si}$ = Dielectric constant, Si

$E_x$ = Electric field strength at distance X

$X$ = Distance from the edge of the conducting region of the lightly doped material.

The potential difference between the conducting region of the lightly doped background material and point X in the junction, is the internal of $E_x$,

$$V = -1/2 \frac{N}{E_{Si}} X^2 \tag{3-4}$$

The ratio of V to $E_x$ at the surface of the heavily doped region where $E_x$ is greatest, is

$$\frac{-V}{E_x} = \frac{X}{2} \tag{3-5}$$

If $E_x$ is the maximum allowable field at point X, and V is the sum of chemical potential difference and applied voltage, then the junction thickness (disregarding sign of V in equation 3-5)

$$X = \omega = 2\frac{V}{E_B} \tag{3-6}$$

For a junction with no applied voltage, $V = V_G = 1.1$ volts. Combining the expressions for $E_B$ and $\omega$ it is possible to find the maximum allowable potential difference across a PN junction vs impurity concentration in the more lightly doped substrate background. The result:

$$V_{max} = 9.8 \times 10^7 \ (N^{-0.4}) \tag{3-7}$$

Similarly, the depletion width $\omega$, containing this maximum potential difference is

$$\omega_{max} = 3.5 \times 10^7 \ (N^{-0.7}) \tag{3-8}$$

The externally applied collector potential of a bipolar transistor must not exceed $V_{max} - V_G$ and the peak operating voltage must be less than this to provide a safety factor. Careful design will permit operating voltages of the order of one volt peak; with a safety factor of 3, $V_{max}$ can have a value of 3 + 1.1 = 4.1 volts. The impurity concentration N, corresponding to this value of $V_{max}$ is $2.8 \times 10^{18}$ atoms/$cm^3$. For this impurity density, the maximum depletion width, $\omega$, would be:

$$\omega_{max} = 3.5 \times 10^7 \ (2.8 \times 10^{18})^{-0.7} = 4.28 \times 10^{-6} \text{ cm} = 428\text{Å} \tag{3-9}$$

This result, in close agreement with the data of Hoeneisen and Mead for an external voltage of 3 volts, is approximately the smallest depletion width feasible for the collector junction of a bipolar transistor. The emitter junction typically operates at less voltage, but cannot be allowed to break down at zero voltage; a similar calculation shows that the emitter depletion width would be approximately 220Å.

A minimum of six PN junctions are encountered, crossing a bipolar device, so that the junctions alone exclusive of the electrode area would comprise 0.216 microns of the device diameter. The electrodes must have adequate thickness (usually 10,000Å) to act as a good conductor at the maximum operating current of the device. The electrode thicknesses must be approximately 500Å, as exposed at the surface, though the emitter electrode might be somewhat smaller, but about 500Å in diameter. Then the electrode surface exposure, exclusive of junctions, would be approximately 2500Å. As a result, a circular planar bipolar device can occupy approximately 0.216 + 0.25 = 0.466 microns in diameter, or an area of approximately $0.2\mu^2$. No isolation margins or safety factors have been included; a practical geometry would necessitate 4 to 5 times the area stipulated.

The conclusions, evident upon the above calculations, indicate that a planar bipolar device must have a minimal area of $1\mu^2$ per device. This dimension is still beyond the capabilities of current photolithographic equipment.

A single gate occupies a much larger area than an individual device, since it requires more than one bipolar device in addition to device contact areas and conductors. The ratio of required gate area to bipolar device area varies with the type of logic. A typical value for $T^2L$ is 5:1, this means that one $T^2L$ gate would occupy an area of $5\mu^2$ per gate. The device termination pad connections, test pads, test devices, etc., actually use up most of the available chip area; only 40 percent of most chip designs are actually occupied by the gate logic geometry. The effective chip area per gate must therefore be increased to $12.5\mu^2$ per gate due to the limiting factors mentioned above.

Bipolar gate density would therefore be estimated at 80,000 gates/$mm^2$ for gates comprised of planar bipolar devices occupying $5\mu^2$/gate. Logic families such as $I^2L$ might achieve higher density than other bipolar families since gates can be made from fewer devices.

Dielectric breakdown between MOS FET gate electrodes and the semiconductor surface is one key limitation in the miniaturization of MOS devices. In order to create a conducting channel near the semiconductor's surface directly under the gate electrode, the surface potential must be depressed by the voltage on the gate electrode ($V_G$). To effect this depression in surface potential, the electric field must be transmitted by the gate electrode through the dielectric layer, which is usually $SiO_2$. The electric field in the oxide is greater than that in the silicon in proportion to the ratio of the dielectric constants of the silicon to that of the oxide or insulator film. As the normal $Si:SiO_2$ ratio is approximately 11.7:3.9, there is a tendency for the oxide to break down long before the field in the silicon reaches its breakdown value. To prevent oxide breakdown, the doping level of the silicon can be reduced, since the field at the silicon surface with a given surface potential can be stipulated as:

$$F_o = [2(V + V_G)Nq/E_{si}]^{1/2} \qquad (3\text{-}10)$$

which varies as the square root of the doping concentration N. The effect of reducing the doping concentration is to increase depletion depth. Since each electrode is surrounded by a depletion region, the spacing between electrodes must be sufficient to prevent any overlap between depletion zones. Hoeneisen and Mead state that minimum electrode spacing is about 5000Å for a 3 volt drain to substrate difference. The minimum area for such a device, considering all other factors in the design of an MOS FET, is approximately 1.5 microns$^2$, not including any margin around source and drain structure. Actually both source and drain are surrounded by depletion regions, typically 5000Å deep; permitting an additional region for channel stop or isolation, the minimum area for a FET is about $6.2\mu^2$. Allowing five transistors per gate, the gate area necessitates $32\mu^2$, corresponding to 31,250 gates/mm$^2$. Assuming that active devices occupy only 40 percent of a MOS chip, there would be only 12,500 gates/mm$^2$; this figure pertains primarily to NMOS logic; CMOS logic would occupy twice the area of NMOS, therefore providing half as many gates per unit of area.

### 3.6.3 Scaling Down to the Ultimate

Scaling down the gate structures of LSIs provides significant advantages other than enabling additional circuit density or enabling a higher level of circuit and/or function integration. Speed of logic functions can be increased without necessarily increasing power dissipation for a chip of specified size. This is extremely important in military or aerospace applications where speed is the prime consideration. A review of the data presented in previous sections indicates that device geometries can be reduced by at least one order of magnitude without encountering any fundamental limitations. Dr. Robert N. Noyce, in an unpublished INTEL Corporation memorandum (Reference 6), stated that a logic gate of an LSI can be reduced in its linear dimensions by a factor of 1/X, subject to the conditions that all electric fields in the device remain constant. This constraint is necessary, since the existing fields cannot be increased by much without the occurrence of avalanche breakdown in either the PN junctions or in the gate insulation of MOS devices.

The thickness of the PN junctions of a bipolar device must scale as X; therefore, to avoid increasing the electric field E, the total voltage V across the junction (internal voltage + supply voltage) must vary directly with X.

$$\therefore \quad V \sim X \tag{3-11}$$

For reduced junction thickness proportional to X, at constant maximum field, the impurity concentration N, throughout the device must vary inversely with X.

$$N \sim \frac{1}{X} \tag{3-12}$$

Current density J, varies directly with the product of the electric field and impurity concentration,

$$J \sim EN \qquad (3\text{-}13)$$

Logic families such as $I^2L$ which operate at very low supply voltages (1.5 volts), cannot be simply scaled down as outlined above. Other limitations of this approach involve miniaturization effects on conductor metallization. To avoid metal migration caused by electro-chemical interaction of contaminant ions with LSI metallization, it is necessary to maintain a minimum conductor thickness of 5,000Å to 10,000Å. The width of such conductors can be scaled down by a factor of X, however, the net result is to insure constant current density in the conductor's cross section. Noyce states that heat is absorbed at a bipolar transistor's emitter, nullifying some of the heat generated at the collector junction, created by internal collector potential $V_o$. Therefore, power dissipation per chip tends to be reduced rather than remain constant with a reduction in device size, if scaling down of a device's geometry is carried out in accordance with the concepts outlined above.

A summary of Factors Affecting Further Reductions in LSI Device Geometries

- The minimum area for a single planar bipolar device is approximately $1\mu^2$
- Assuming a 40 percent utilization factor for an LSIs surface area and assuming an average of five bipolar devices per gate, a chip of one $mm^2$ could accommodate a maximum of 80,000 bipolar gates
- The minimum area of a planar FET is approximately $6.25\mu^2$
- Assuming a 40 percent utilization factor for an LSIs surface area and assuming an average of five MOSFETs per gate, a one $mm^2$ chip can accommodate a maximum of 12,500 MOS gates
- CMOS devices can provide a maximum of approximately 6,250 gates
- DCCL cannot be compared directly with NMOS or CMOS logic, however, a comparison of digital building block circuits indicate that DCCL occupies approximately one half the area needed for the same logic function in dynamic NMOS
- Potential increases in device densities are approximately 100 times greater than current device densities.

# 4. SUMMARY AND RECOMMENDATIONS

This section summarizes the requirements for high speed A/D converters in comparison with the corresponding capabilities of the five technologies covered. The development needs of the two most promising technologies are summarized, and specific A/D and A/D technology developments are recommended.

## 4.1 SUMMARY OF SYSTEM REQUIREMENTS

The A/D requirements discussed in the system requirements study of Section 2 are plotted, by application in Figure 4-1. Requirements of size, weight, and power are generally of secondary importance in all but spacecraft applications. Cost requirements dominate wherever high quantities of A/D converters are involved. Figure 4-1 shows three clusters of requirements that can be grouped by sample rate. The low sample rate group includes all requirements below 10 Msps. The medium sample rate group includes all requirements from 25 to 250 Msps. The high sample rate group includes all requirements above 250 Msps.

Table 4-1 gives the practical A/D solution to these requirements in silicon bipolar and GaAs FET technologies. All of the requirements 500 Msps and below can be met with silicon A/D implementations, with 1 Gsps and above requiring GaAs FET or other technology for solution. However, if power consumption is important many of the higher speed silicon A/D converters may no longer be considered practical; e.g., a 250 Msps, 8 bit silicon A/D converter currently in development requires 60 watts. Any A/D requirements can be satisfied by a GaAs FET implementation at less than one-tenth the power achieved with silicon bipolar. This power savings and the higher sample rate ability make GaAs FET technology attractive.

## 4.2 SUMMARY OF A/D TECHNOLOGY CAPABILITIES

A performance projection for high speed A/D converters produced in the five technologies discussed in this report is given in Table 4-2; additional comparison information is given in Table 4-3.

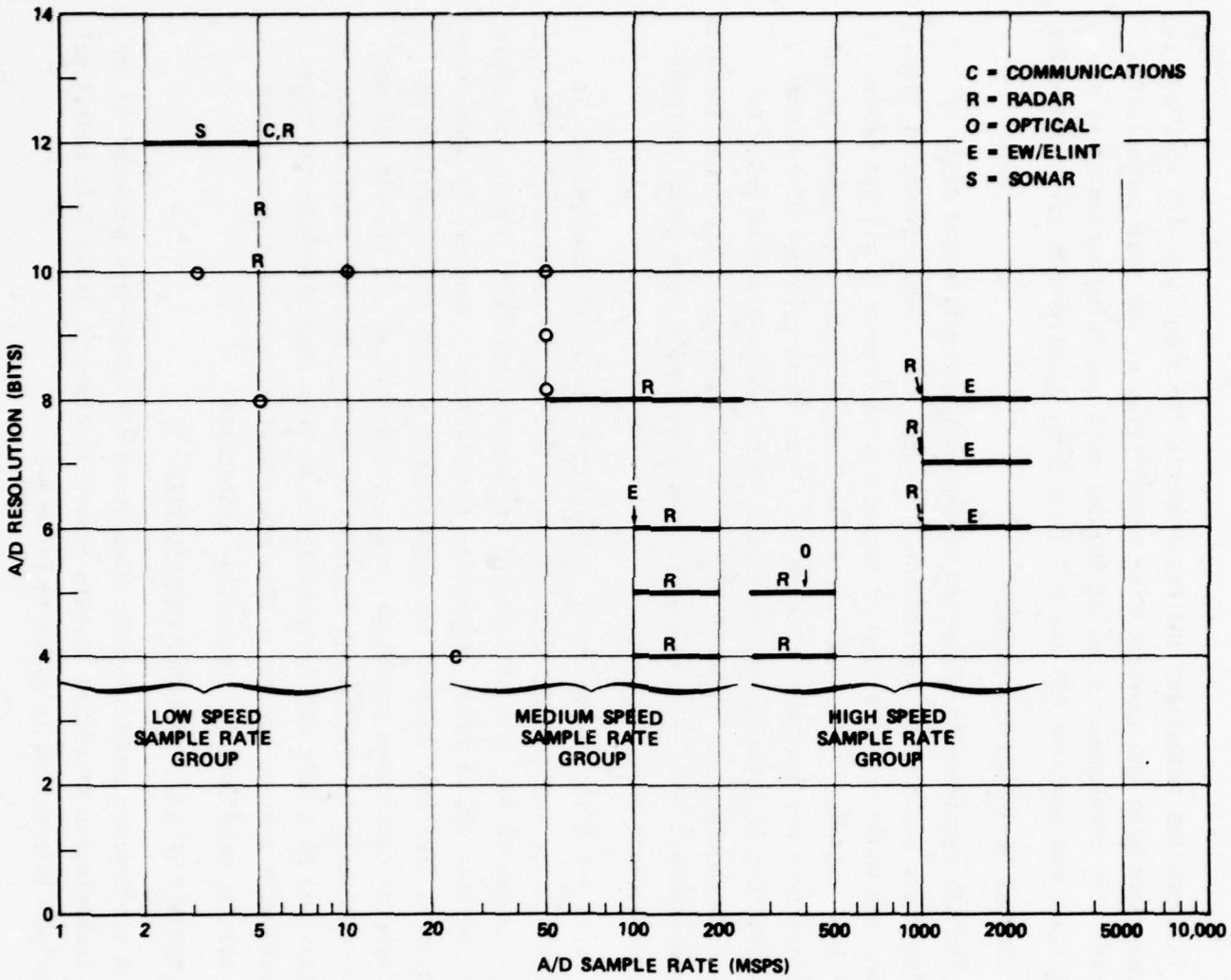


Figure 4-1. A/D Requirements by Application

Table 4-1. A/D Requirements Versus Capabilities

| SAMPLE RATE GROUP | RESOLUTION RANGE (BITS) | SILICON | GaAs FET |
|---|---|---|---|
| LOW (1 TO 10 MSPS | 8 TO 12 | 5 MSPS 12 BIT<br>10 MSPS 10 BIT | 10 MSPS 12 BIT |
| MEDIUM (25 TO 250 MSPS) | 4 TO 10 | 50 MSPS 10 BIT<br>250 MSPS 8 BIT | 80 MSPS 10 BIT<br>250 MSPS 8 BIT |
| HIGH (250 TO 2500 MSPS) | 5 TO 8 | 400 MSPS 5 BIT<br>1000 MSPS AND ABOVE NOT PRACTICAL | 1000 MSPS 8 BIT<br>2500 MSPS MAY BE POSSIBLE IN 5 YEARS |

## Table 4-2. Performance Projection of High Speed A/D Technologies

| TECHNOLOGY | ADVANTAGES | LIMITATIONS | POTENTIAL CAPABILITIES | | STATE-OF-ART A/D CONVERTERS | | | STATUS | COMMENTS |
|---|---|---|---|---|---|---|---|---|---|
| | | | SPEED AT 8 BITS | MAXIMUM ACCURACY (BITS) | MSPS | BITS | WATTS | | |
| SILICON BIPOLAR TRANSISTORS | • HIGH ACCURACY<br>• HIGH SPEED<br>• EXISTING LSI TECHNOLOGY | • MODERATE POWER | 500 MSPS | 16 | 5<br>10<br>10<br>20<br>50<br>250<br>400 | 12<br>10<br>13<br>8<br>10<br>8<br>5 | 5<br>4<br>70<br>4<br>2.5<br>60<br>20 | PROPOSED (TRW)<br>EXISTING (TRW)<br>EXISTING (COMPUTER LABS)<br>EXISTING (TRW)<br>IN DEVELOPMENT (TRW)<br>IN DEVELOPMENT (HUGHES)<br>EXISTING (TRW) | ALL SAMPLE RATES WILL DOUBLE IN NEXT 5 YEARS AT SAME BITS AND POWER AS A RESULT OF ELECTRON BEAM MASKING |
| GALLIUM ARSENIDE FET | • HIGH ACCURACY<br>• HIGH SPEED<br>• LOW POWER<br>• MONOLITHIC SAMPLE AND HOLD | • TECHNOLOGY DEVELOPMENT REQUIRED | 2 GSPS | 16 | 50<br>80<br>300<br>1000<br>1000 | 12<br>10<br>8<br>6<br>8 | 0.15<br>0.15<br>0.30<br>0.40<br>1.20 | PROPOSED (TRW)<br>PROPOSED (TRW)<br>PROPOSED (TRW)<br>PROPOSED (TRW)<br>PROPOSED (TRW) | BEST TECHNOLOGY FOR NEAR-TERM DEVELOPMENT (3 TO 5 YEARS) OF ADVANCED A/D CONVERTERS. ALL CONVERTERS ARE COMPLETE SINGLE CHIP A/D'S INCLUDING ON-CHIP SAMPLE AND HOLD CIRCUITS |
| GALLIUM ARSENIDE TED | • VERY HIGH SPEED<br>• LOW POWER | • TECHNOLOGY DEVELOPMENT REQUIRED<br>• LOW ACCURACY | 10 GSPS | 6 | 5000<br><br>10,000<br>10,000 | 1 (CASCADABLE CELL)<br><br>4<br>5 | 0.30<br><br>1.0<br>1.5 | IN DEVELOPMENT (TRW)<br><br>PROPOSED (TRW)<br>PROPOSED (TRW) | REQUIRES GaAs PROCESS THAT CAN PRODUCE FET's AND TED's ON SAME LSI CHIP |
| JOSEPHSON JUNCTION | • VERY HIGH SPEED<br>• LOWEST POWER<br>• MONOLITHIC SAMPLE AND HOLD | • CRYOGENIC TEMPERATURES<br>• TECHNOLOGY DEVELOPMENT REQUIRED<br>• LOW ACCURACY | 50 GSPS | 8 | 62.5 | 4 | - | EXISTING (IBM) | NEEDS LIQUID HELIUM TEMPERATURE BUT OFFERS EXTREMELY LOW POWER |
| ELECTRO-OPTICAL | • HIGH SPEED | • MODERATE POWER<br>• TECHNOLOGY DEVELOPMENT REQUIRED<br>• LOW ACCURACY<br>• LARGE SIZE<br>• HIGH WEIGHT | 2 GSPS | 8 | 250<br><br>2000<br><br>1000 | 8<br><br>6<br><br>6 | -<br><br>-<br><br>7.3 | DEVELOPMENT UNSUCCESSFUL (EBS DEVICE)<br>IN DEVELOPMENT - EBS DEVICE (WATKINS-JOHNSON)<br>IN DEVELOPMENT - LASER DEVICE (NOSC) | LARGE SIZE AND WEIGHT RELATIVE TO SOLID STATE APPROACHES |

Table 4-3. Comparison of High Speed A/D Technologies

| TECHNOLOGY | SIZE AND WEIGHT | RELIABILITY | RADIATION HARDNESS | AVAILABILITY | COST |
|---|---|---|---|---|---|
| SILICON BIPOLAR | SINGLE LSI CHIP TO HYBRID COLLECTION OF 2 TO 20 CHIPS | VERY HIGH AND WELL SUBSTANTIATED (MTBP $10^7$ HOURS) | VERY HARD $10^7$ RAD (Si) | EXCELLENT | VERY LOW ($100 TO $10K) |
| GALLIUM ARSENIDE FET | SINGLE LSI CHIP TO HYBRID OF A FEW CHIPS | SHOULD BE HIGH BUT NOT YET PROVEN | VERY HARD; LEVELS NOT DETERMINED | ANTICIPATE GOOD AVAILABILITY AS PROCESSING MATURES | LOW ($500 TO $10K) |
| GALLIUM ARSENIDE TED/FET | SINGLE LSI CHIP TO HYBRID OF A FEW CHIPS | SHOULD BE HIGH BUT NOT YET PROVEN | VERY HARD; LEVELS NOT DETERMINED | ANTICIPATED LIMITED AVAIL-ABILITY DUE TO LIMITED APPLI-CATIONS | LOW ($500 TO $10K) |
| JOSEPHSON JUNCTION | SMALL LSI CHIP REQUIRES CRYOGENIC COOLING APPARATUS | UNKNOWN | UNKNOWN | ANTICIPATE POOR AVAIL-ABILITY DUE TO EXPENSIVE DEV-ELOPMENT COSTS | HIGH COST DUE TO CRYOGENIC REQUIREMENTS |
| ELECTRO-OPTICAL | BOTH EBS AND LASER APPROACHES HAVE LARGER SIZE AND WEIGHT THAN SOLID STATE APPROACHES EXCEPTING JOSEPHSON JUNCTION DUE TO COOLING APPARATUS | LOW FOR EBS UNKNOWN FOR LASER APPROACH | UNKNOWN | ANTICIPATE LIMITED AVAIL-ABILITY DUE TO LIMITED APPLICATIONS | UNKNOWN |

## Silicon Bipolar

Silicon bipolar is the only technology that has produced useful A/D converters. A/D converters in silicon run the gamut from a printed circuit board full of transistors and integrated circuits to single chip LSI A/D converters. Eight different single chip quantizers have been produced by TRW Systems during the last 4 years. One popular compromise is to use a thin film cermaic or polyimide substrate to mount and interconnect from 2 to 20 silicon IC devices in achieving a complete A/D converter. Over the next 5 years smaller geometry devices made possible by electron beam masking will allow the speed of all existing and proposed silicon bipolar converters to double at the same resolution and power consumption. The recent advent of silicon monolithic high speed sample-and-hold circuits will allow complete single chip A/D converters (S/H plus quantizer) to be built eliminating the need for separate costly hybrid sample-and-hold circuits.

## Gallium Arsenide

Gallium arsenide FET process development is under way at several aerospace companies. Most of the work is aimed at integrated FET circuits with a few companies also interested in TED devices. Several of these companies have an interest in high speed GaAs A/D converter development. A distinct advantage of GaAs is the ease with which the sample-and-hold function can be implemented (particularly in comparison with silicon bipolar). GaAs requires further process development to achieve the LSI complexity level required by a complete A/D converter.

## Josephson Junction

The IBM Corporation is the acknowledged leader in Josephson junction technology. They have developed an experimetal 62.5 Msps 4 bit A/D converter. Josephson junction technology offers incredible sampling rate potential (50 Gsps) at resolution up to 8 bits. The principal drawbacks are the need for cryrogenic cooling, and reliability uncertainty (some devices do not survive exposure to room ambient temperatures).

Electro-Optic

The two forms of electro-optic A/D conversion are limited in resolution to about 8 bits. Since these approaches use either an EBS vacuum tube or a laser light source, the physical size and weight is considerably higher than any solid state approach, with the exception of Josephson junction and its associated cooling apparatus.

## 4.3 RECOMMENDATION

Silicon bipolar and gallium arsenide FET are the two technologies that have the most significant potential for satisfying present and future naval A/D system applications.

Although silicon bipolar is a well established technology, it still has significant growth potential. Application of LSI complexity silicon bipolar technology to high speed A/D converters was started in 1974 with a successive approximation algorithm quantizer. More complex series-parallel and full-parallel organizations are just beginning to surface as initial design implementations. Considerable potential for advances in performance exists as a result of improved circuit and algorithm designs. However, the greatest advance in silicon bipolar LSI anticipated in the near term future (3 to 5 years) will come as a result of electron beam masking. The basic advantage of electron beam lithography is finer resolution of photoresist, and therefore, finer device geometries. The practical advantages of finer device geometries include:

1) Higher frequency capability

2) Larger number of dice per wafer

3) Higher yields or the capability to maker larger LSIs with reasonably high yields

4) Lower power requirements.

The advantages of primary interest to high speed A/D converters are higher frequency capability, lower power requirements, and the capability to make larger LSIs with reasonable yields. It is anticipated that speed and power capabilities will be increased by a factor of 2 with the application of electron beam lithography.

Gallium arsenide FET integrated circuits offer excellent potential for future high speed A/D converters. GaAs ICs are presently being fabricated with SSI complexity and gigahertz operating frequency. The feasibility of this technology for high speed IC is evident from published results on GaAs FET circuits and processes.

Large scale GaAs integrated circuits for digital and analog applications require developments in materials, devices, and process technology to achieve reliable circuits with high performance levels. The aspects of development include improvements in performance, reliability, and producibility (repeatability of specific parameters at an acceptable yield). The performance requirements include achievement of higher frequency operation and lower power dissipation in analog and logic circuits. These are achieved with smaller geometries and specific control of material parameters. Additionally, uniform material parameters and device geometries are required for close matching of neighboring devices. These parameters are achieved with conventional epitaxial materials and with ion-implanted structures. For reliability considerations, ion-implanted planar structures are being developed, although mesa FETs with shallow epitaxial layers (less than 0.2 μm) may be just as reliable and provide better isolation.

The optimum configuration for achieving small size, low power, and high performance is a single monolithic chip implementing of the A/D function. The low interconnect capacitance and neglishable inductance allows the circuits to perform at the limit of the individual device capabilities. Future systems in radar, optical, Elint, and Sonar will require large numbers of A/D converters to process signals from arrays of detectors. Single chip monolithic fabrication has the atributes of being maintenance and adjustment free and low cost in production.

### 4.3.1 Recommended Programs Using Existing Technology

All of the low and medium sample rate range requirements can be satisfied with silicon technology. In some cases the required A/D converters are already in development. Several of these developments are severely straining the capability of current silicon technology. The drawback of pushing existing technology too far is excessive power consumption, high recurring cost, and low performance compared to theoretical. Two examples

of this are the Aeroflex 800 Msps 6 bit A/D converter in which eight 100 Msps full-parallel A/Ds, constructed from commercial comparators, are time interleaved to obtain the high sample rate. This A/D takes well over 100 watts of power and has an inherently high recurring cost due to the high parts count. The A/D can be replaced with a single chip GaAs 6 bit 1 Gsps A/D converter requiring less than 1 watt of power.

The second example is the 250 Msps 8 bit A/D being developed by Hughes Aircraft. This unit uses sixteen 4 bit quantizer chips for a full-parallel 8 bit quantizer and requires 60 watts of power. The recurring cost is expected to be high due to the large number of custom chips on a hybrid substrate plus the parts and assembly cost of the hybrid sample-and-hold circuit and combining logic. How close these units are to theoretical performance is unknown. High performance and low cost are always easier to achieve when the requirements are well within the technology capabilities.

Without overstressing the silicon technology capabilities, three A/D converters are recommended to be developed that will have low power consumption, low recurring cost, and closely approach theoretical performance. These three A/D converters fully cover the low and medium sample rate groups. No attempt has been made to prioritize these developments as each services a different group of applications. All three silicon A/D converters can be developed as single chip monolithic quantizers with a thin film hybrid sample and hold circuit. In each case the complete A/D can be developed in approximately 18 months. Upon completion of the high speed monolithic sample and hold development work, under AFAL Contract F33615-78-C-1428, the technology capability will exist to combine the monolithic quantizer with a monolithic sample and hold and produce complete single chip monolithic A/D converters.

The first of these is a 12 bit 5 Msps A/D. This converter can be developed as a single chip successive approximation quantizer with a thin film hybrid sample and hold. The quantizer chip can be included in the hybrid package resulting in a single package complete A/D converter. Power consumption is estimated at 4 watts. This A/D, in conjunction with a 10 Msps 10 bit A/D converter, will meet all of the A/D requirements in the low sample rate group. A breadboard 10 Msps 10 bit A/D converter has been built and tested by TRW Defense and Space Systems Group using a single chip silicon

quantizer (developed on AFML Contract No. F33615-75-C-5135) and a thin film hybrid sample-and-hold circuit.

The second recommended silicon A/D development is a 10 bit 50 Msps A/D. This converter can be developed as a single chip series-parallel silicon quantizer with a thin film hybrid sample and hold. As in the preceding A/D, the quantizer chip can be included in the hybrid package resulting in a single package complete A/D converter. Power consumption is estimated at 3 watts. This development will satisfy the 10 bit requirement in the low and medium sample rate groups.

The third recommended silicon A/D development is a 6 bit 250 Msps A/D converter. This A/D can be developed as a single chip full parallel quantizer. For some applications the chip can be used without a sample-and-hold circuit, and the quantizer chip would then be the complete A/D converter. Power in this case is estimated at 3 watts. For near theoretical performance on high input signal frequencies a hybrid or monolithic sample-and-hold circuit would be required, adding approximately 2 watts to the above power. A fallout of this development would be a 250 Msps 8 bit A/D converter with lower power and parts count than the 8 bit, 250 Msps A/D previously mentioned. Four 6 bit quantizer chips, hybrid sample-and-hold circuit, and combining logic chip (previously developed by TRW on AFAL Contract No. F33615-73-C-1218) could be assembled in a single package to form the complete A/D converter. The power is estimated to be a total of 16 watts.

These 6 and 8 bit A/D converters and the 10 bit 50 Msps A/D together will meet all of the requirements in the medium sample rate group (25 to 250 Msps), for near term applications. In the long run a GaAs FET solution for the 8 bit 250 Msps A/D requirement should be sought for reduced power and lower recurring cost.

The capabilities of existing plus recommended silicon A/D converters is shown in Figure 4-2, overlaid on the Naval A/D requirements.

### 4.3.2 Recommended A/D Technology Development Programs

Gallium arsenide FET technology is projected to be capable of fabricating LSI A/D converters with a megasample per watt ratio from 10 to 30 times higher than silicon. Recommendations for GaAs A/D development revolve

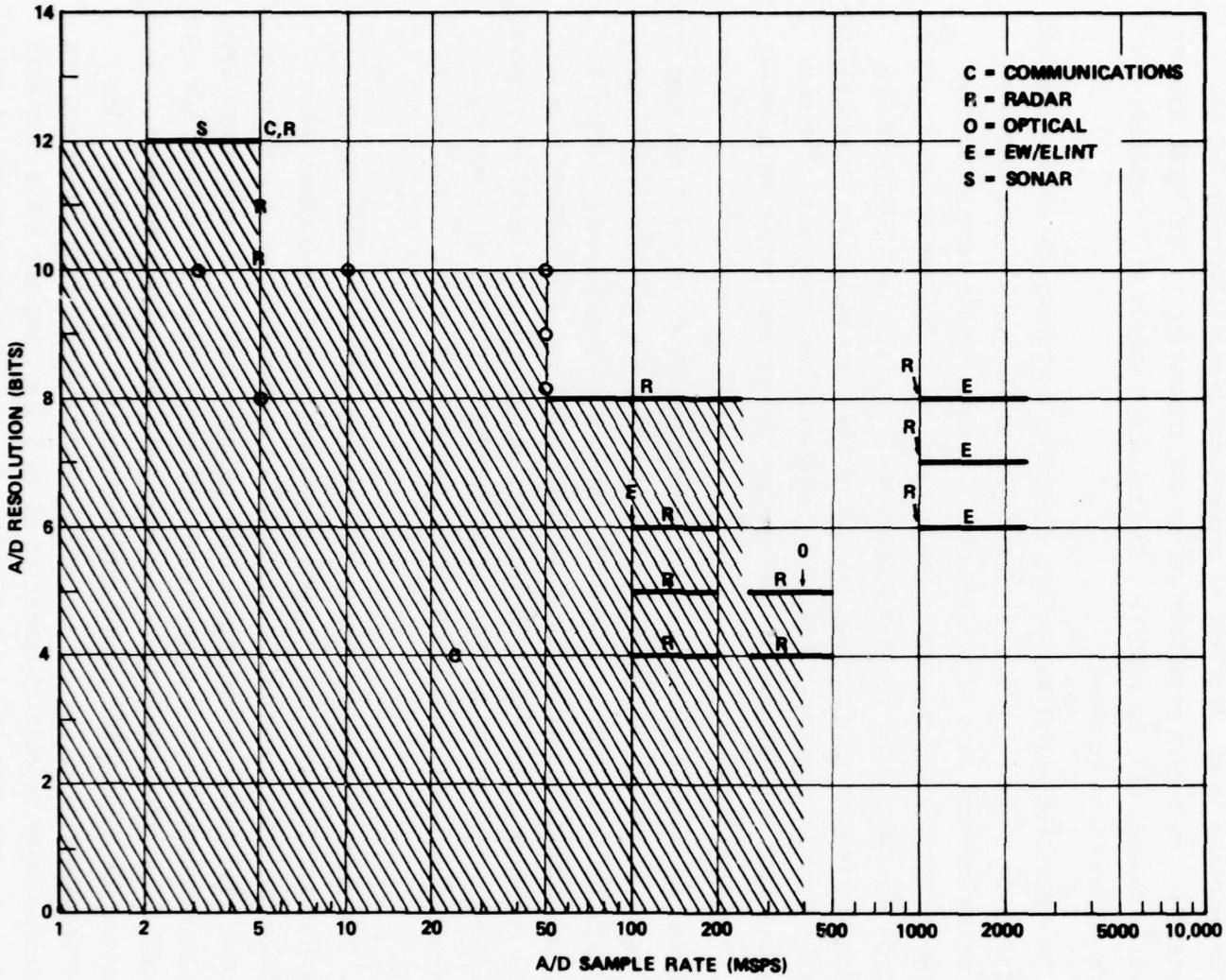


Figure 4-2. Silicon A/D Converter Technology Capabilities Overlaid on Naval A/D Requirements

around three classical high speed A/D organizations: successive approximation, series-parallel, and full-parallel. Preliminary design calculations have been made for each organization using a 2 micron geometry FET. This device geometry is at the limit of present day photolithography for LSI complexity. As E-beam mask fabrication and processing is developed smaller geometry devices will be possible, projected A/D speeds will increase, and power consumptions decrease.

A successive approximation A/D converter, including the sample-and-hold circuit, can be fabricated as a single chip complete A/D. This converter can be implemented as a 12 bit A/D with a maximum sample rate of 50 Msps and would require 150 mW power. The A/D would have 800 devices on a single 60 x 80 mil chip. This one development would satisfy the 50 Msps 10 bit medium sample rate requirements and all of the low sample rate group requirements. A 10 bit version of this design has also been examined. The chip size and power are essentially the same but the maximum sample rate would increase to 80 Msps.

The recommended series-parallel monolithic A/D is an 8 bit 300 Msps converter. The A/D can be organized as a two stage 4 bits/stage feed-forward organization. The A/D can be implemented on a single LSI chip, including sample and hold, and is projected to require 300 mW. The reduced size and power compared to the 8 bit 250 Msps silicon A/D converter under development should be of great interest for future systems. This A/D will satisfy all of the medium speed group Naval A/D requirements for 8 bit or less resolution.

The third recommended GaAs converter development utilizes the full-parallel A/D organization. This is the highest speed and highest power approach to A/D conversion, requiring $2^N - 1$ comparators for an N bit resolution. The number of conversion bits is determined by how many comparators can be integrated onto a single monolithic chip, traded off against how much speed is lost if multiple chips are required. Preliminary designs have been examined for 6 and 8 bit single chip full-parallel A/D converters. The power consumption is 0.4 and 1.2 watts, respectively. Both converters are estimated to be capable of operation up to 1 Gsps, and the 6 bit chip with process improvements (including electron beam masking or processing) will

operate up to 2.5 Gsps. These two full parallel A/D developments will satisfy nearly all of the high speed sample rate group requirements.

The potential capabilities of GaAs A/D converters overlaid on Naval A/D requirements is shown in Figure 4-3. All of the current and projected requirements can be satisfied with the exception of the 8 bit 2.5 Gsps EW/ELINT application. It is prudent to wait for further device, circuit, and process development before making any projection of this extreme in performance.

The silicon and gallium arsenide developments recommended in this study focus on single monolithic chip quantizers and A/D converters. There is a significant performance advantage of producing all of the resistors and transistors of a complete A/D quantizer simultaneously on a single monolithic chip. This is due to the matching and temperature tracking of the device characteristics combined with the exceptionally low and predictable parasitic capacitances and negligible inductances inherent in the construction. Achieving LSI levels of integration in GaAs is even more important than in silicon due to the device and parasitic capacitances being more than an order of magnitude lower in GaAs than in silicon. Only a fraction of the speed · power advantage of GaAs over silicon is realized with the SSI levels of integration currently in development in GaAs.

Gallium arsenide processing capabilities are currently below the LSI level required for these A/D converters, therefore any A/D technology development program should be planned to include process and device development as well as individual circuit, and finally complete A/D development work. Of the three A/D converter organizations the successive approximation and full-parallel algorithms are the easiest to implement. Development of a series-parallel A/D should wait until both of these organizations have been built. Implementation of high speed digital processing functions are equal in importance to the A/D developments discussed here, and require the same technology. Figure 4-4 illustrates the structure and schedule for a multiphase GaAs A/D and digital function development program. During the initial phase, process and device development work would be pursued to assure that all of the devices anticipated for the Phase II and III developments get designed, processed, and tested. Most of the focus of Phase I is on devices, device modelling, and processing. Also during this phase, all of the circuits required for Phases II and III should be built and evaluated. During

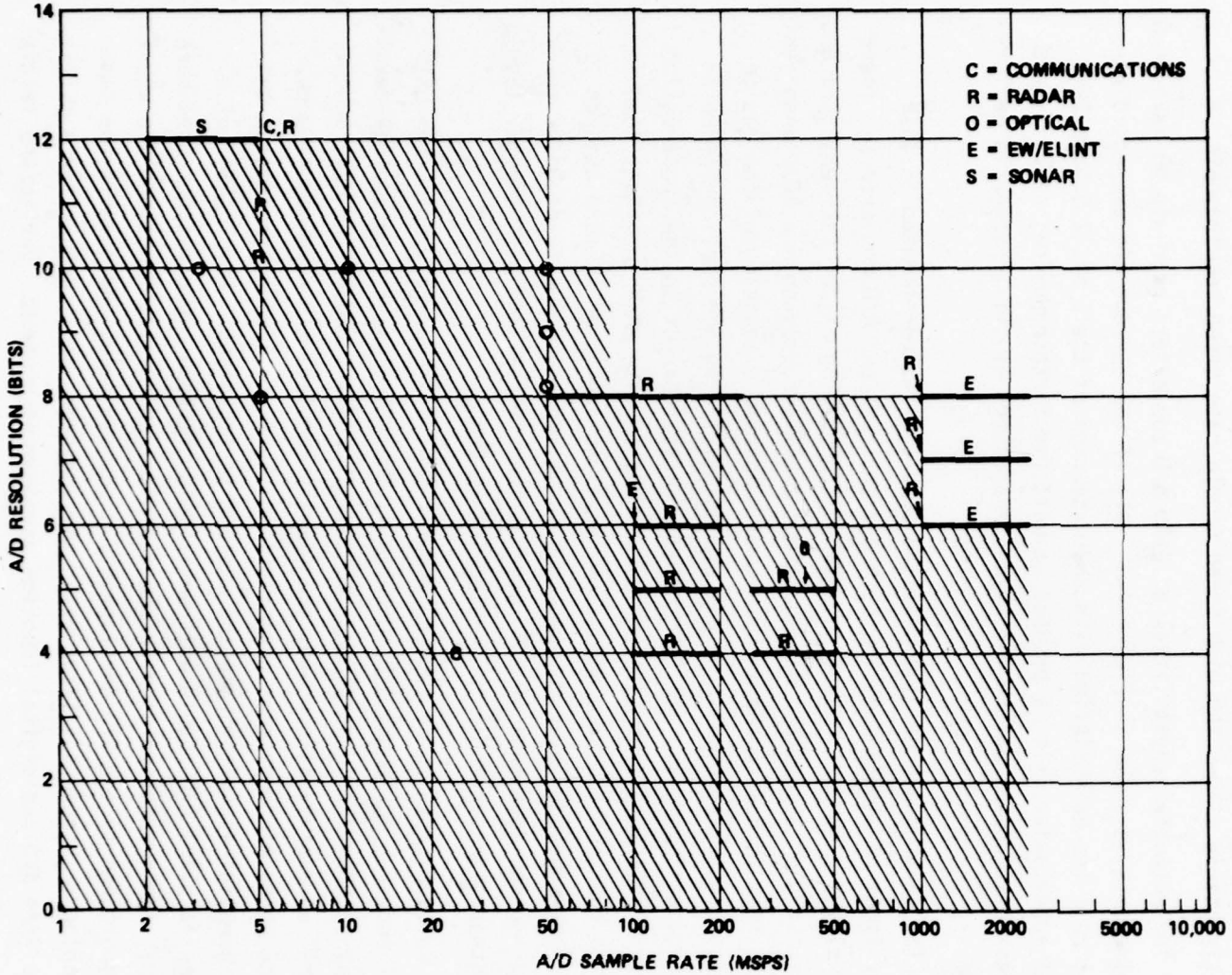


Figure 4-3. Gallium Arsenide FET A/D Converter Capabilities Overlaid on Naval A/D Requirements

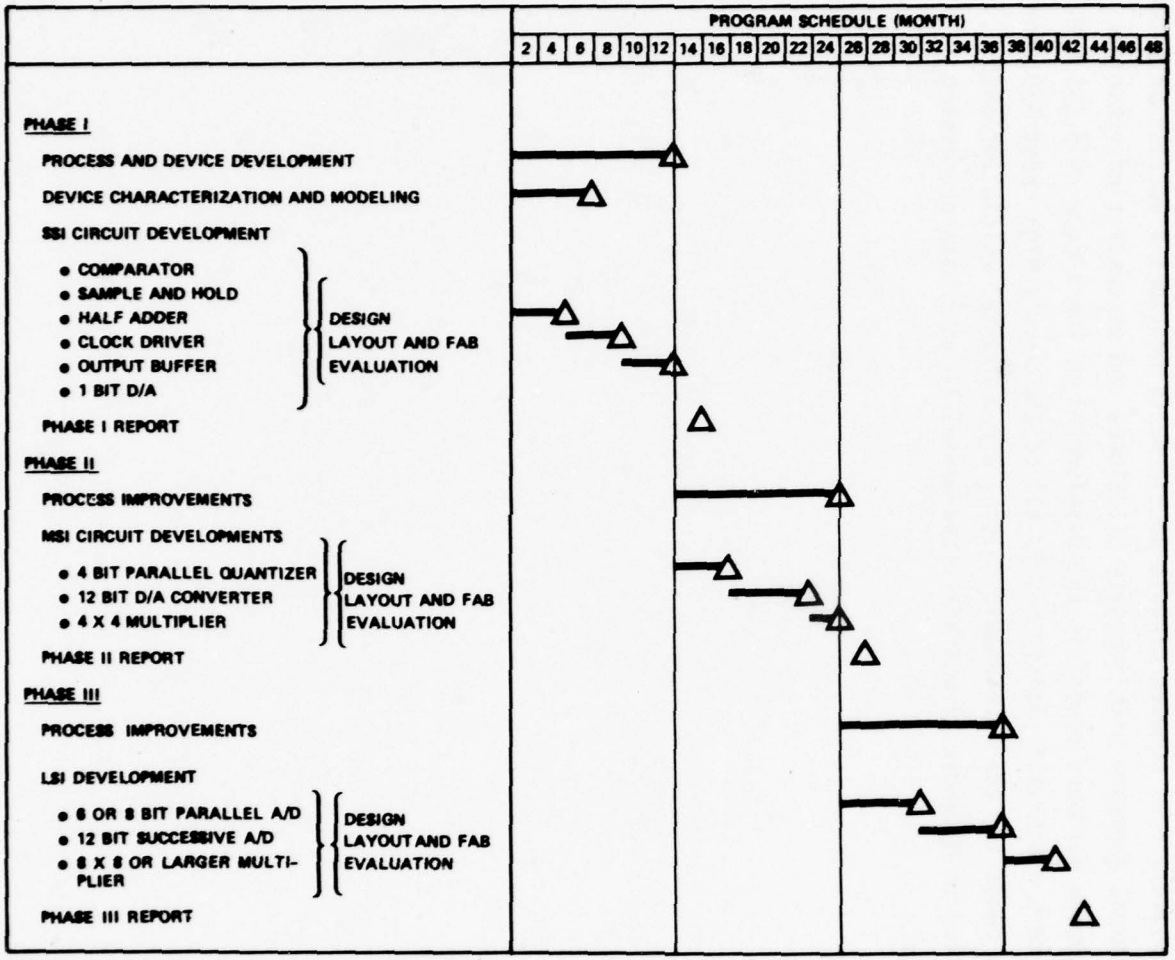


Figure 4-4. Recommended GaAs Development Program

Phases II and III processing work continues in improvements and refinements to build the foundation for MSI and LSI process capability. Three MSI circuit developments are recommended in Phase II. Each circuit is the next logical step leading to the Phase III LSI developments. The three-phase program with continuous process development and refinements paralleled by progressively more complex circuit developments provides a success oriented development approach with adequate milestones and demonstration vehicles. The program hardware payoff is the development of two single chip LSI A/D converters which will satisfy nearly all of the Navy's high speed A/D converter needs for the foreseeable future, and a digital multiplier chip (detailed in Appendix A) which is fundamental to most data processing systems.

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# APPENDIX A

## GALLIUM ARSENIDE FET TECHNOLOGY

The gallium arsenide FET technology is an emerging technology which offers excellent potential for achieving low delay-power product and high speed. This technology appears equally well suited to the implementation of high speed interface circuits (e.g., analog to digital converters), as well as digital signal processing functions (i.e., ALUs, multipliers, etc).

Because of the emerging status of the GaAs FET technology, Section A-1 presents an introduction to the circuit technology and discusses approaches for achieving the optimum configuration for low delay power and high speed. Section A-2 presents a preliminary design for a 12 bit 50 Msps A/D converter, which illustrates the potential for achieving efficient analog and digital circuitry in Gallium Arsenide. This section also describes a 10 bit 200 Msps converter. Section A-3 presents the design of a 16 bit parallel multiplier which is capable of performing 100 million multiplies/sec. This design illustrates the potential high speed and low power of GaAs logic designs.

### A.1 BASIC GaAs CIRCUIT CONSIDERATION

This section discusses the rationale for a GaAs FET approach to high speed, low power digital and analog circuitry. The low parasitic capacitances that are principally responsible for the low delay-power products projected for GaAs integrated circuitry are examined. Direct coupled logic employing enhancement mode devices is reviewed as are various current mode logic schemes. This latter circuit form, particularly in a differential logic implementation, is far less sensitive to the device gate voltage characteristics and can use either enhancement, depletion, or a device whose characteristics are in between these two modes; thereby, promising higher processing yield than other logic forms.

Analog circuit considerations are discussed, including enhancement vs depletion modes, implementation and characteristics of current generators, and the effects of finite gate currents plus a wideband operational amplifier.

#### DIGITAL CIRCUIT CONSIDERATIONS

The advantages of enhancement mode FET devices for high speed, low power logic applications appear to be significant. Moreover logic circuits using enhancement mode FET's do indeed provide an excellent speed-power product (0.002 pj). However, it will be shown here that the propagation delay of enhancement mode FET circuits (>5 nsec) is substantially larger than the propagation delay required for 100 MHz arithmetic functions and A/D converters (propagation delay ≈ 0.1 to 1.0 nsec).

A differential current mode logic circuit approach is presented that achieves the required gate delays to allow high speed arithmetic and A/D functions to be realized with low system power.

Parasitic Capacitances

The greatest single advantage of GaAs over silicon for achieving low delay-power product logic is the low parasitic capacitance that results from the use of an insulating substrate. The GaAs substrate is typically 10 mils (254 microns) thick. If this substrate were mounted on a metallic package bottom, the capacitance of pads and lines to the case bottom would be higher than if a glass or ceramic carrier were inserted between the GaAs chip and the case bottom. This kind of assembly could purposely be done for a single chip circuit or would naturally occur in a hybrid circuit assembly including the GaAs chip as one add-on component. The calculations here are for the chip attached directly to a metallic case and thereby represent a worst case capacitance. The capacitance of several pertinent geometric shapes is given below for use in following sections.

Capacitance of a Pad to Substrate Bottom

The capacitance of a small conductive pad such as a source, gate, or drain is estimated from the capacitance of two equal size oppositely changed spheres.*

$$C = 2\pi \varepsilon_0 \varepsilon_r a \sinh \beta \sum_{N=1}^{\infty} \cosh N\beta$$

where

$\varepsilon_0 = 8.85 \times 10^{-12}$ farad/meter

$\varepsilon_r = 12.5$ (GaAs)

a = radius of sphere

$\cosh \beta = \frac{r}{2a}$

r = distance between centers of spheres

The capacitance resulting from this expression is half that from one sphere to a plane located half way between the spheres and normal to a straight line between the sphere centers. The sphere represents a small pad and the plane is the bottom of the substrate. An effective dielective $\varepsilon_r = 8$ is used to make allotment for the split dielective as shown in Figure 1. The capacitance of a 4 by 4 micron pad is 0.9 femto farad ($0.9 \times 10^{-15}$ farad).

*American Institute of Physics Handbook, 1972, pp. 5-12 to 5-18.

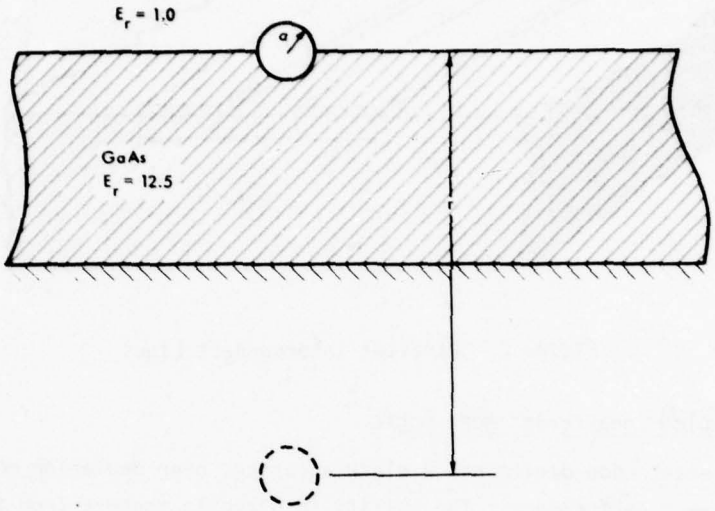



Figure 1. Sphere Over A Ground Plane

*Capacitance of a Line to Substrate Bottom*

The capacitance of an interconnect line to the substrate bottom is calculated from microstrip transmission line equations with the aid of impedance and propagation velocity curves calculated from the works of Wheeler.* The capacitance obtained for a 4 μm wide line, 10 mils (254 μm) long on a 10 mil GaAs substrate is 15.6 femto farads.

Capacitance between Adjacent Lines

The capacitance between adjacent parallel lines as shown in Figure 2 is given as

$$C = \frac{2\,\varepsilon_o \varepsilon_r K\{k\}}{K\sqrt{1-k^2}}$$

where

$\varepsilon_o = 8.85 \times 10^{-12}$ farad/meter

$\varepsilon_r = 12.5/2$ (GaAs/Vacuum)

$$k = \sqrt{\frac{ab}{(a+c)\,(b+c)}}$$

and $K\{k\}$ is the complete elliptic integral of modulus k. For two 4 μm wide lines separated by 4 μm and running parallel for 10 mils the capacitance is 22 femto farads.

*The Microwave Engineer's Handbook and Buyers Guide, 1968, pp. 94-95.

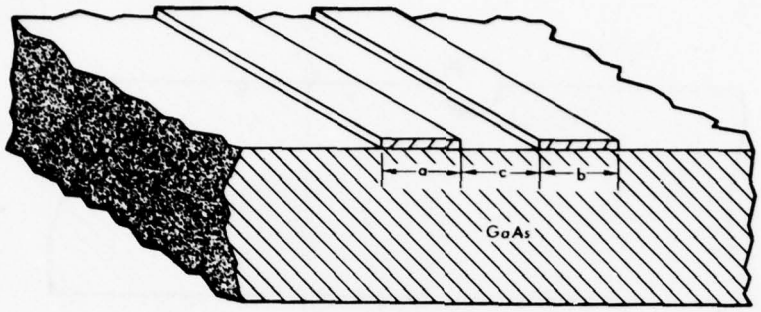



Figure 2. Parallel Interconnect Lines

Direct Coupled Enhancement Mode Logic

The enhancement mode device has a clear advantage over depletion mode for obtaining low delay-power performance. The ability to directly connect from the drain of one device to the gate of the next, as illustrated in Figure 3, is key to the delay-power advantage, allowing direct coupled logic circuits. Enhancement mode devices require only a single low valued power supply whereas logic circuits using depletion mode devices require either level shifting, a bias voltage, or two supply voltages. The voltage swing for switching an enhancement mode device from off to on is smaller than that required for a depletion mode, further reducing power. The gate source junction on the enhancement device in direct coupled logic clamps the upper logic level and ground (zero volts) sets the lower logic level, allowing simple gate structures and uniform logic levels.

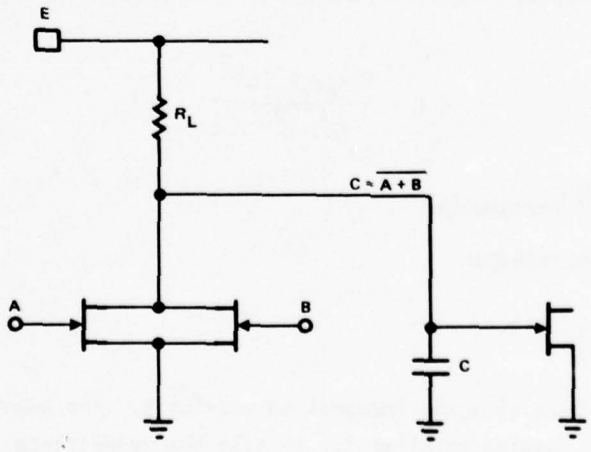



Figure 3. Direct Coupled Logic Using Enhancement Mode FET

Logic Gate Configurations

The simplest gate configuration for enhancement mode Schottky gate FET logic is the direct coupled circuit of Figure 3. The load resistor $R_L$ must be considerably larger than the on channel resistance to assure the lower logic output level is low enough to cut off the gate input of the following device. This creates two greatly different time constraints at the gate drain node which translate into different gate delays for output rise and fall transitions. This difference is minimized by increasing the power supply voltage, which increases the gate power. The rise time delay of the gate (Figure 3) is given by

$$T_{d_r} = R_L \, C \, \ln \frac{E - V_0}{E - V_T}$$

and the fall time delay is given by

$$T_{d_f} = R_{ON} \, C \, \ln \frac{V_1 - V_0}{V_T - V_0}$$

where

$R_L$ = gate load resistor

C = total load capacitance device + resistor + parasitic

E = supply voltage

$V_0$ = logic "0" voltage

$V_T$ = logic threshold voltage

$R_{ON}$ = FET on resistance

$V_1$ = logic "1" voltage

The fall time delay expression can be simplified since

$$V_1 - V_o = 2 \times (V_T - V_0) \text{ to}$$

$$T_{d_f} = R_{ON} \, C \, \ln 2$$

$$T_{d_f} = 0.7 \, R_{ON} \, C$$

The lower output logic level is

$$V_0 = I_L \, R_{ON} = \frac{E}{R_L} R_{ON}$$

and $$\frac{R_L}{R_{ON}} = \frac{E}{V_O}$$

The cutoff voltage for the enhancement mode device is +100 mV. Therefore, to leave some noise margin, a lower logic level ($V_0$) of +50 mV is chosen.

The upper logic level ($V_1$) is determined by the clamp action of the forward biased gate and is +500 mW for the design value gate current density. The mid point or threshold level of the gate input voltage is therefore approximately +300 mV.

Since the supply voltage (E) must be higher than the upper logic level (500 mV), the ratio of $R_L$ to $R_{ON}$ must be

$$\frac{R_L}{R_{ON}} = \frac{E}{V_o} \geq \frac{500}{50} = 10$$

$$\frac{R_L}{R_{ON}} \geq 10$$

Returning to the delay equations

$$T_{d_r} = R_L C \ln \frac{E - V_o}{E - V_T}$$

$$T_{d_f} = 0.7 R_{ON} C$$

Taking the ratio of rise delay to fall delay we get

$$\frac{T_{d_r}}{T_{d_f}} = \frac{R_L C \ln \frac{E-V_o}{E-V_T}}{0.7 R_{ON} C}$$

$$\frac{T_{d_r}}{T_{d_f}} = 1.4 \frac{R_L}{R_{ON}} \ln \frac{E-V_o}{E-V_T}$$

A plot of

$$\frac{T_{d_r}}{T_{d_f}} \text{ vs } E \text{ with } \frac{R_L}{R_{ON}} = 10,\ V_o = 50 \text{ mV},\ V_T = 300 \text{ mV}$$

is given in Figure 4. From the plot we see that the rise delay is dominant. From the expression for the fall delay we see that it is independent of supply voltage. Therefore we proceed with a calculation of the rise delay times power product. The result is plotted in Figure 5. From the plot we see that the lowest supply voltage obtains the lowest delay power product and (from Figure 4) the worst delay ratio for rising vs falling transitions.

It is clear at this point that the best delay-power product is obtained when operating at the minimum supply voltage (600 mV). The required ratio of $R_L/R_{ON}$ has been shown to be

$$\frac{R_L}{R_{ON}} = \frac{E}{V_0}$$

Evaluating this expression with E = 600 mV and $V_0$ = 50 mV, we get $R_L/R_{ON}$ = 12.

The basic enhancement mode geometry under consideration has the following characteristics for a 4 μm width:

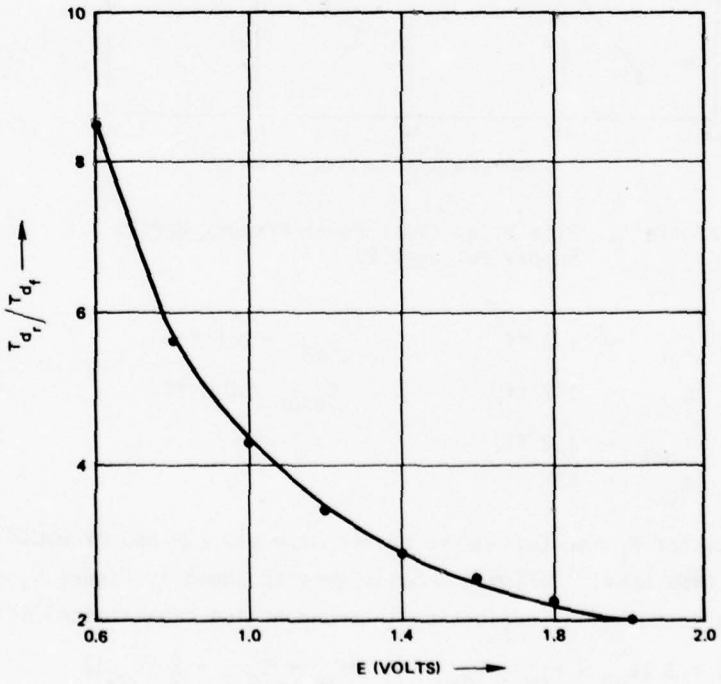



Figure 4. Ratio of Rise Delay to Fall Delay Versus Supply Voltage E for a Constant $R_L$

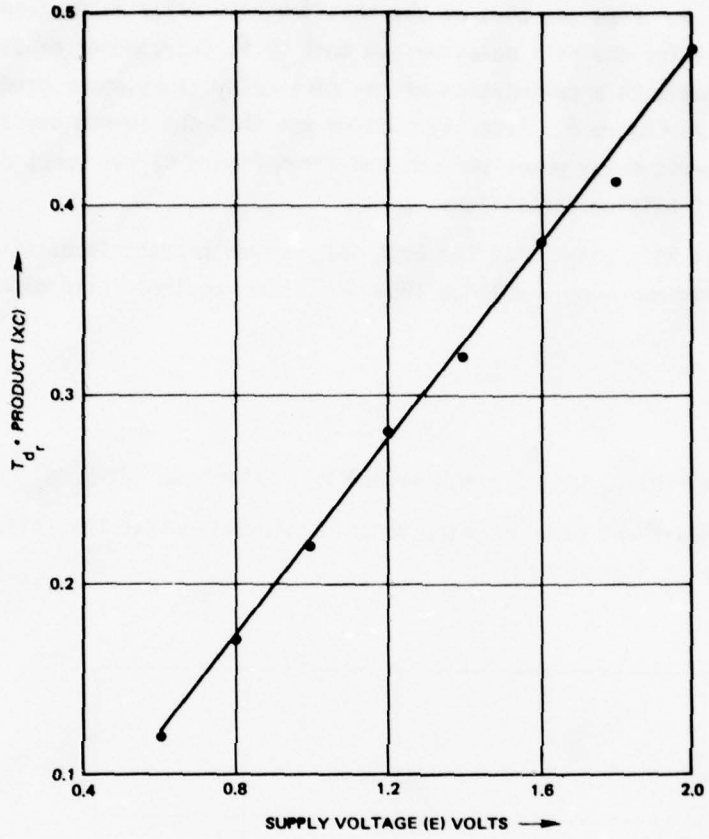



Figure 5. Rise Delay Times Power Product Versus Supply Voltage (E)

$C_{gs}$ = 1.2 ff $C_{sd}$ = 0.5 ff

$C_{gd}$ = 1.2 ff $C_{dsub}$ = 0.9 ff

$C_{gch}$ = 1.2 ff

$R_{ON}$ = 45K

The load resistor $R_L$ for this basic device size and E = 600 mV would therefore be $R_L = 12\ R_{ON}$ = 540K ohms. Defining a basic gate as shown in Figure 6, the load capacitance for a fanout of 3 (neglecting interconnecting capacitance) is

$$C = 3\ (C_{gd} + C_{sd} + C_{dsub}) + 3\ (C_{gs} + C_{g_{ch}} + 2\ (C_{gd}))$$

C = 22.2 femto farads

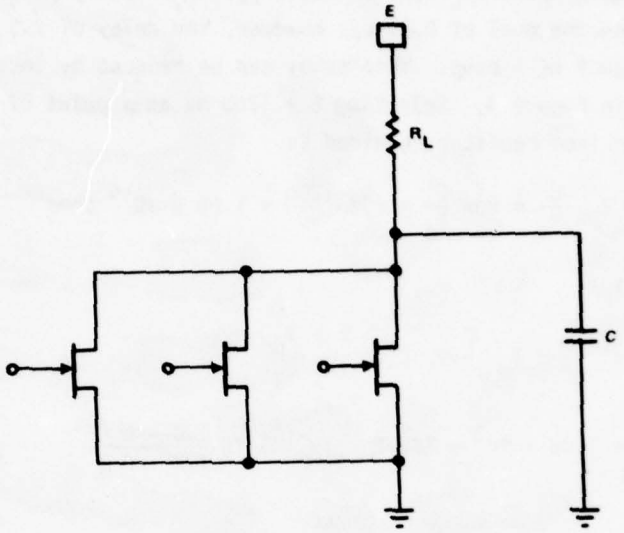



Figure 6. Basic Three Input Gate Configuration

The gate delay which is determined by the rise delay is

$$T_{d_r} = R_L \, C \, \ln \frac{E - V_o}{E - V_T}$$

$$T_{d_r} = 540K \, (22.2 \times 10^{-15}) \, \ln \frac{0.6 - 0.05}{0.6 - 0.3}$$

$$T_{d_r} = 7.3 \text{ nsec}$$

and the power dissipation is

$$P = E \, \frac{E - V_T}{R_L}$$

$$P = 0.6 \, \frac{0.6 - 0.3}{540K}$$

$$P = 0.33 \times 10^{-6} \text{ watts}$$

This results in a delay power product of 0.002 pj. This delay power product is a factor of 5 better than the goal of 0.01 pj; however, the delay of 7.3 nsec is worse than the maximum goal of 1 nsec. This delay can be reduced by increasing the supply voltage as seen in Figure 4. Selecting E = 1200 mV as a point of diminishing returns, the load resistor required is

$$R_L = R_{ON} \frac{E}{V_o} = Ron \frac{E}{V_o} = 45K \frac{1200}{50} = 1.08 \times 10^{+6} \text{ ohms}$$

The gate rise delay is

$$T_{d_r} = R_L \, C \ln \frac{E - V_o}{E - V_T}$$

$$T_{d_r} = 1.08 \times 10^6 \times (22.2 \times 10^{-15}) \ln \frac{1.2 - 0.05}{1.2 - 0.3}$$

$$T_{d_r} = 5.9 \text{ nsec}$$

The delay does not decrease as rapidly as predicted by Figure 4 due to the requirement to increase $R_L$ with E so as to maintain the lower logic level.

From these brief analyses, it is clear that direct-coupled GaAs enhancement mode FET logic is too slow for extremely high speed A/D converters and arithmetic circuits. Further disadvantages can be noted regarding the tight process controls required to achieve uniform enhancement and pinchoff characteristics. Moreover, the wide variation of propagation delay between rising and falling transitions, plus the system inefficiency of the low power supply voltage required, suggests additional drawbacks to this approach.

Current Mode Logic

Current mode logic gate configurations are considered next as a means of obtaining the required gate delays of 0.1 to 1.0 nsec. These circuits can use enhancement, depletion, or devices with a gate voltage vs drain current characteristic in between. The optimum device characteristic will be investigated early in the program. The following current mode gates are evauated with a depletion mode FET identical to that employed in the analog circuit and A/D converter sections.

A straightforward current mode MESFET logic gate is illustrated in Figure 7. The circuit uses a depletion mode FET (X1) with the following characteristics:

| | | | |
|---|---|---|---|
| $C_{gs}$ | = 1.2 ff | $R_s$ | = 2.1K |
| $C_{gd}$ | = 1.2 ff | $R_d$ | = 2.1K |
| $Cg_{ch}$ | = 1.2 ff | $R_{ON}$ | = 5.9K |
| $C_{sd}$ | = 0.5 ff | Vp | = -0.52 V |
| $C_{dsub}$ | = 0.9 ff | $I_{DSS}$ | = 45 μA |
| | | Gm | = 107 μmhos |

Where X2 or X4 appears on the schematic, a wider device with 2 or 4 time higher capacitance, transconductance and $I_{DSS}$, and 1/2 or 1/4 the indicated resistance is intended.

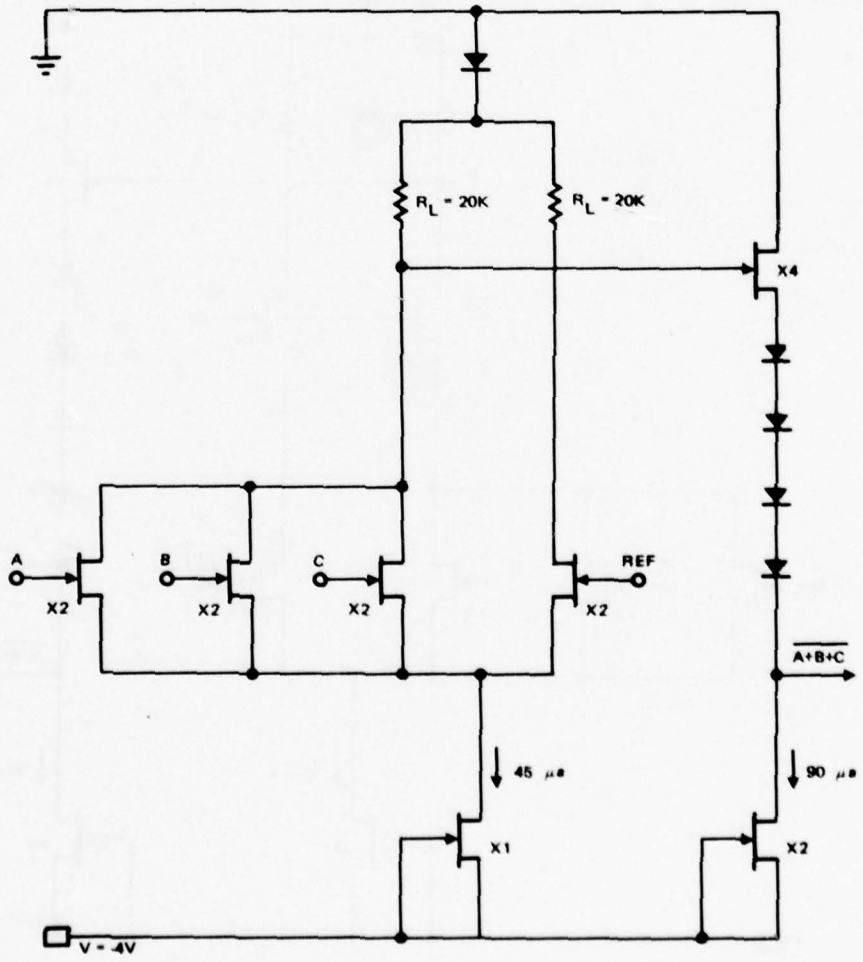



Figure 7. Current Mode NOR Gate

The circuit has an estimated delay, driving a fanout of 3 but neglecting interconnect capacitance, of 221 psec at a gate power of 0.54 mW, for a delay power product of 0.12 pj. An improvement can be made to this circuit by adding a common gate FET between the three input device drains and $R_L$ as shown in Figure 8. This reduces the Miller effect on the input capacitance, thereby reducing the gate delay to 113 psec. However, an additional level shift diode is required, raising the supply voltage to -4.5 V and increasing the gate power to 0.61 mW. The net change is a reduction in delay-power product to 0.07 pj. Either of these circuits can supply a complementary output signal with the addition of a second level shift circuit driven by the unused load resistor at an expense in power of 0.36 to 0.40 mW and no increase in delay to either output.

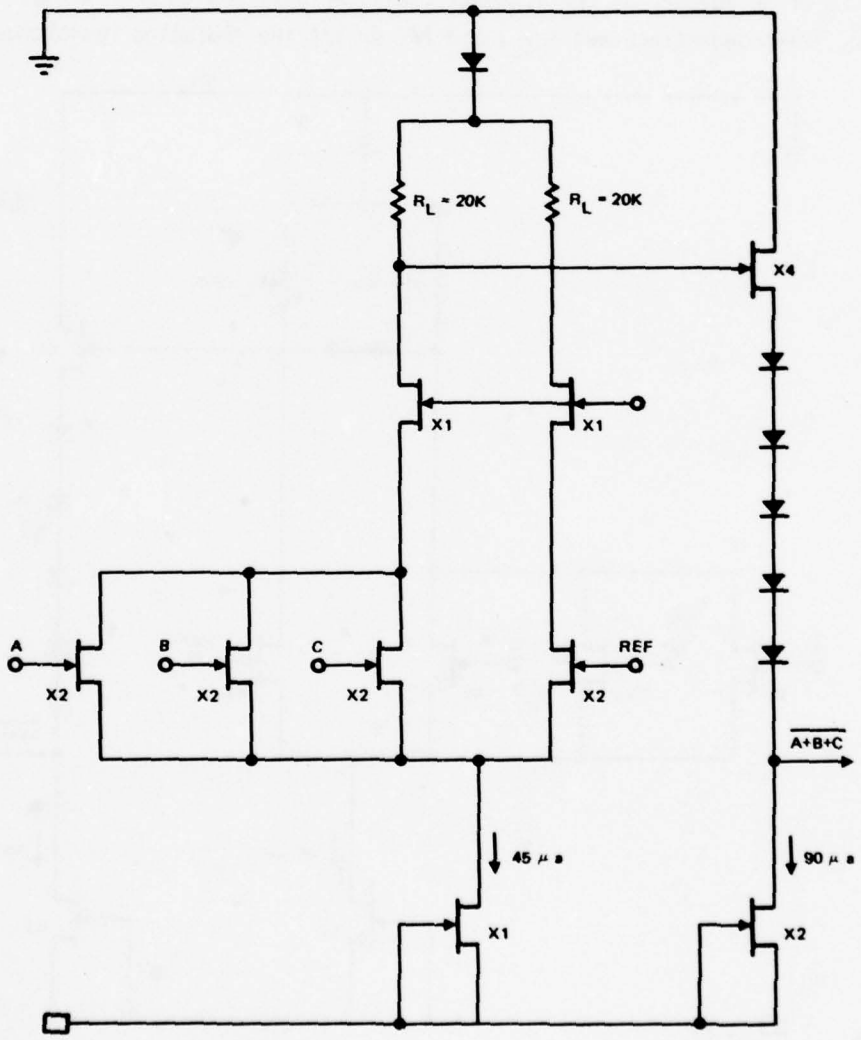



Figure 8. Modified Current Mode Gate

Differential Current Mode Logic

Another form of current mode logic employs differential signals with half the swing required for single-ended current mode logic. This reduced swing gives the circuit an inherent improvement of 2 in delay-power product. The differential nature of the logic simultaneously provides both true and complementary signals. The vertical nature of the gating conserves power while allowing complex gating functions to be achieved in a single circuit. An example of a differential gate circuit is shown in Figure 9. This simple circuit forms the complex logic function $A\,C + B\,\overline{C}$. The delay of this gate to the lower output driving a fanout of 3 but neglecting interconnect capacitance is 114 psec. The gate power is 0.47 mW and delay power product per gate term is 0.018 pj or 0.54 pj for the complete circuit.

The differential current mode logic concept performs several logic functions per single circuit. The concept can be expanded both vertically and horizontally to from more complex logic functions. Figure 10 is one such example where an exclusive-OR and a latch flip-flop have been combined into a single circuit. An even more complex circuit can be found in the full adder described for the 16 x 16 multiplier in Section 3, where due to the increased logic complexity the equivalent gate count increases to the point that a delay-power product less than 0.01 pj is achieved.

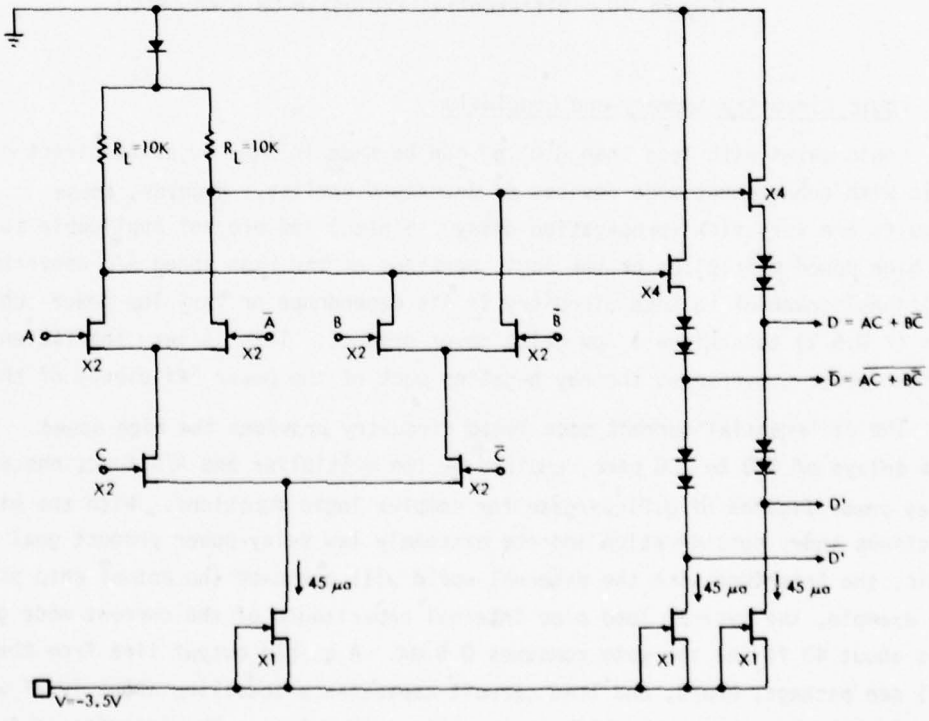



Figure 9. Differential Current Mode Logic Gate

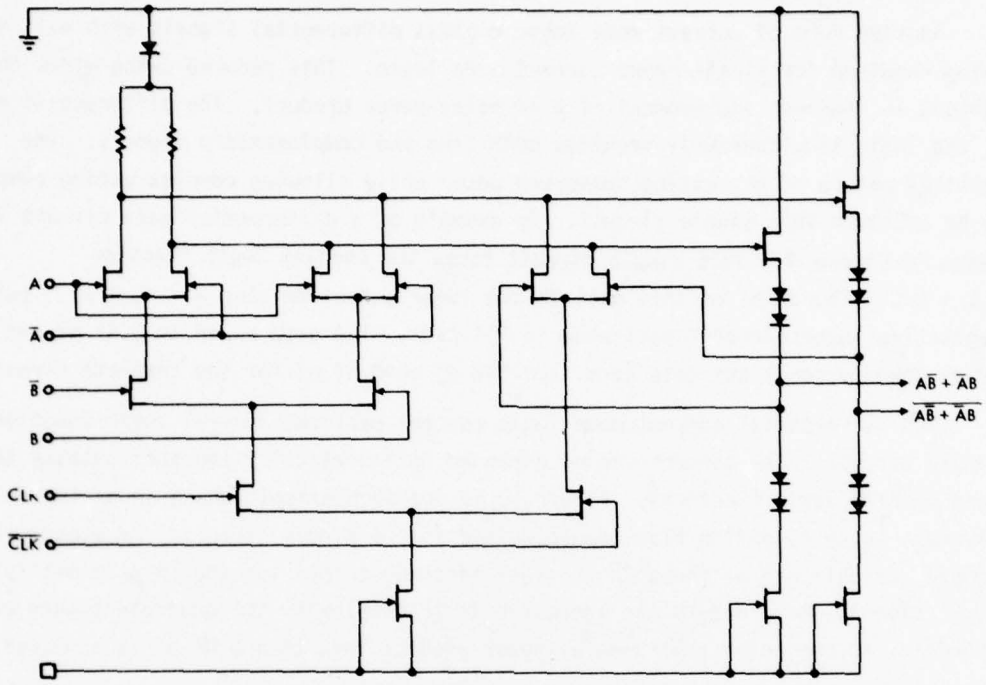



Figure 10. Differential Exclusive OR with Latch

Logic Circuitry Summary and Conclusions

Logic gates with less than 0.01 pj can be made in GaAs by using direct coupled logic with enhancement mode devices as described earlier. However, these circuits are very slow (propagation delay 5 nsec) and are not applicable to either the high speed multiplier or the logic portions of the high speed A/D converter. One additional drawback to such circuitry is its dependence on very low power supply voltages ($\approx$ 0.5 V) to achieve a low delay power product. This is very inefficient for present power converters, thereby negating much of the power efficiency of the logic.

The differential current mode logic circuitry provides the high speed gate delays of 100 to 200 psec required by the multiplier and A/D functions and achieves delay power figures of 0.01 pj/gate for complex logic functions. With the high speed functions under consideration and the extremely low delay-power product goal for the logic, the interface with the external world will dominate the actual chip power. For example, the typical load plus internal capacitance of the current mode gates runs about 40 ff and the gate consumes 0.5 mW. A single output line from the chip will see package, board, and load circuit capacitance totalling about 10 pF which is 250 times higher than that which the on-chip gate drives. The interface driver would

therefore consume ≈ 250 x 0.5 = mW per output if the 100 to 200 psec delay were required. In most applications, 100 to 200 psec delay times are not required and the power can be reduced. However, the interface power will still be considerable, if not dominant in most circuits built with such low delay-power logic. For example, the output drivers in the A/D discussed in Section 3 use 48 mW of the total A/D power of 75 mW. Further improvements in the on-chip logic delay-power product will tend to be masked by the interface circuit power consumption.

TRW has used silicon bipolar differential current mode logic in all of its LSI monolithic developments for the past 3 to 4 years. Included in this are a 16-bit digital correlator, an 8 x 8 parallel multiplier, a dual 9-bit parallel-serial multiplier, and seven A/D quantizer chip developments. The versatility of this logic form and ease of design and layout has been proven.

The differential nature of the signals reduces noise generation and susceptibility both on-chip and in the system as a whole. In units incorporating both analog and digital signal, noise considerations make differential logic circuitry virtually imperative.

ANALOG CIRCUITRY CONSIDERATIONS

This section addresses the applicability of enhancement versus depletion mode FET's to analog circuit applications. A wideband operational amplifier design is also presented as an example of a typical analog function.

Enhancement Versus Depletion Mode FET

A comparison between enhancement and depletion mode devices comes out almost totally in favor of the depletion mode device. The only possible advantages of using an enhancement mode FET for any analog circuit are a small reduction in the power supply voltage due to the smaller (300 mV versus 500 mV) gate voltage swing required to control the device, and the ability to direct couple the devices for a small signal amplifier.

The following points all favor depletion mode operation over enhancement mode.

- The transconductance to capacitance ratio for a depletion mode device is approximately 5 times higher than for an enhancement mode device. This results in a correspondingly higher gain-bandwidth product for the device and any circuits built with them.

- Current generators, which are key to both analog and digital circuits, are simply made by shorting the gate-to-source together for a depletion mode device. This results in a 2-terminal current generator which can either source or sink current. Additionally, by changing the device width or adding a resistor in series with the source lead, any value of current can be generated (source or sink). With the N channel enhancement mode device, only current sinks can be made and even these are a 3-terminal circuit requiring a gate voltage bias circuit to complete the generator.

- Gate current is important in several analog circuits such as analog comparators, precision current generators, current switches, and the postamplifier in a sample and hold circuit. Depletion mode devices operate with the gate junction reversed biased and thereby experience only leakage current in the gate. The enhancement mode device, however, operates with the gate source junction forward biased and the gate therefore draws current similar to base current in a bipolar transistor. This gate current is a nonlinearity, error source, or droop in the above named circuits.

One final advantage is that the depletion mode FET can be used for both digital and analog circuits allowing a single monolithic device and process to be utilized for all analog and digital functions. This compatibility is essential in functions employing both analog and digital circuitry such as A/D and D/A converters.

The GaAs depletion mode FET has several desirable advantages over other depletion mode FET's for analog amplification:

- High mobility and much lower device-to-substrate capacitance relative to silicon
- Low input (gate current) errors relative to bipolar technologies
- Large relatively-linear input voltage range relative to bipolar technologies, and also relative to silicon FET technologies due to the gm-linearizing effect of velocity saturation in GaAs
- Low noise broadband amplification from very low frequencies to very high frequencies compared to other technologies
- Radiation-hardened relative to bipolar technologies
- Potentially higher chip temperatures than silicon.

Wideband Amplifier

Wideband amplifiers are normally required ahead of high speed A/D converters used to digitize RF or other low level signals. The system approach normally chosen is to process the RF or low level signal in one assembly, then transmit the signal via a low impedance cable to the A/D assembly. Maintaining low signal levels in such low impedance interconnections is essential if the driving amplifier power consumption is to stay reasonable. Immediately ahead of the S&H in the A/D converter, a wideband low noise amplifier, such as the one discussed in this section, is employed to increase the signal amplitude to the level required by the A/D converter. These amplifiers exhibit open-loop gain-bandwidth products up to 2 Ghz in the silicon hybrid circuit implementations and are used as subtraction amplifiers in feed-forward A/D converter organizations, as both preamplifier and postamplifiers in certain S/H organizations, and as wideband amplifiers to boost low level RF signals to the voltage level required for A/D conversion.

A representative for wideband operational amplifier is shown in Figure 11. As indicated in Tables 1 and 2 of this figure, the concept offers potential closed-loop bandwidths up to 2.5 GHz at 10 mW or less operating power. Estimated phase margin is greater than 40° at 2.5 GHz, yielding reasonable damping (no excessive oscillatory transients) even with the output shorted to the input (e.g., voltage-followers application).

The majority of the power dissipation is associated with the load-driving circuitry. Therefore, total power consumption can be reduced well below 10 mW for light-load applications: especially for on-chip LSI applications where load resistances tend to be very large and load capacitances in the tens of femto farads.

The unusually high 2.5 GHz bandwidth (for a unity-gain-stable operational amplifier) is obtained by a parallel feed-forward concept used in silicon hybrid operational amplifiers designed and manufactured by TRW for the past 5 years.

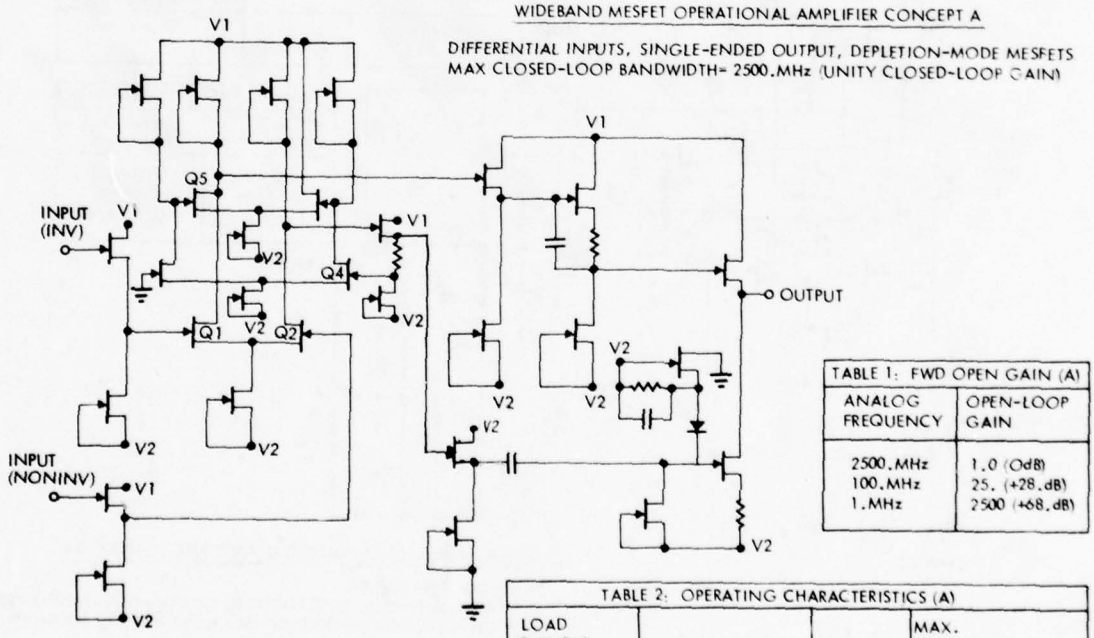



TABLE 1: FWD OPEN GAIN (A)

| ANALOG FREQUENCY | OPEN-LOOP GAIN |
|---|---|
| 2500.MHz | 1.0 (0dB) |
| 100.MHz | 25. (+28.dB) |
| 1.MHz | 2500 (+68.dB) |

TABLE 2: OPERATING CHARACTERISTICS (A)

| LOAD R AND C TO GROUND | | INPUT AND OUTPUT VOLTAGE RANGE | SUPPLY VOLTAGES | MAX. INTERNAL $P_{DISS}$ (OUTPUT=FULL SCALE 100MHz SINEWAVE) |
|---|---|---|---|---|
| R | C | | | |
| 2.KΩ MIN | 3.pf MAX | ± 1.0V | $V_1$=+5V $V_2$=-2V | 6.mW |
| 5.KΩ MIN | 1.2pf MAX | ± 2.56V | $V_1$=+8V $V_2$=-3.5V | 10.mW |

Figure 11. Op-Amp Concept A

The key to obtaining good damping in conjunction with such high closed-loop bandwidth is minimizing the number of inverting-amplifier stages in the forward path of the operational amplifier; the minimum number required is one, as is utilized in this concept (Q1 of Figure 11). The necessary high gain (for good closed-loop accuracy) is then obtained by means of a "2-inverting-stage" amplifier (Q2 and Q3 of Figure 11) placed in parallel with the high-frequency "single-inverter" amplifier.

Figure 12 and associated Tables 3 and 4 describe the same concept with an alternate output driver for delivering high analog output currents to an off-chip low-impedance load such as a transmission line. Use of the high current driver results in a small sacrifice in total power (10 mW rather than 6 mW for ±1 V signal range) and in a maximum stability closed loop bandwidth (1.5 GHz rather than 2.5 GHz).

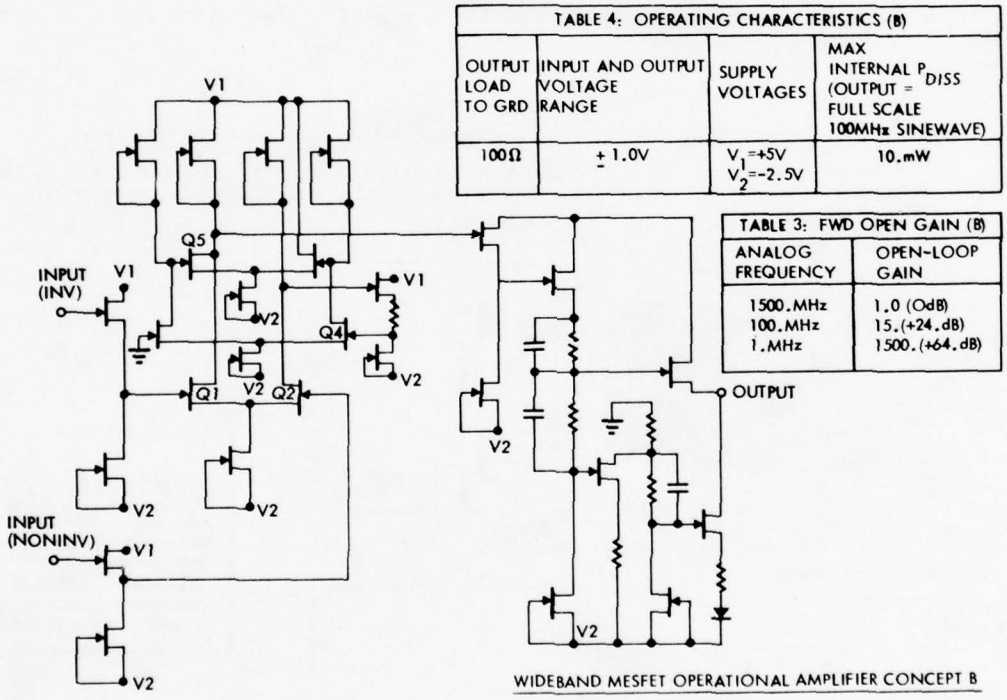



TABLE 4: OPERATING CHARACTERISTICS (B)

| OUTPUT LOAD TO GRD | INPUT AND OUTPUT VOLTAGE RANGE | SUPPLY VOLTAGES | MAX INTERNAL $P_{DISS}$ (OUTPUT = FULL SCALE 100MHz SINEWAVE) |
|---|---|---|---|
| 100Ω | ± 1.0V | $V_1$=+5V $V_2$=-2.5V | 10.mW |

TABLE 3: FWD OPEN GAIN (B)

| ANALOG FREQUENCY | OPEN-LOOP GAIN |
|---|---|
| 1500.MHz | 1.0 (OdB) |
| 100.MHz | 15.(+24.dB) |
| 1.MHz | 1500.(+64.dB) |

WIDEBAND MESFET OPERATIONAL AMPLIFIER CONCEPT B

*HIGH-CURRENT OUTPUT*
DIFFERENTIAL INPUTS, SINGLE-ENDED OUTPUT, DEPLETION-MODE MESFETS
MAX CLOSED-LOOP BANDWIDTH=1500.MHz (UNITY CLOSED-LOOP GAIN)

Figure 12. Op-Amp Concept B

## A.2 A/D CONVERTER

One excellent application for GaAs FET technology is the fabrication of high speed, high accuracy, and low power, monolithic A/D converters. Several different A/D converter circuit configurations can be used, each resulting in a different combination of performance parameters. The final selection of the optimum A/D organization is dependent on the relative importance of speed, accuracy, and power consumption in the desired application.

In this section, two different A/D converter designs based on GaAs depletion-mode FET technology are discussed. The two designs are a 50 Ms/sec, 150 mW, 12 bit successive approximation A/D; and a 200 Ms/sec, 300 mW, 10 bit feed forward A/D. Either design could be developed in a 3 year technology program.

### SUCCESSIVE APPROXIMATION A/D

A block diagram for a successive approximation A/D converter is shown in Figure 13. This approach uses a comparator and D/A converter in a feedback loop to determine the digital value of the analog input by a trial and error technique.

The conversion period is divided into a number of short cycles by timing logic and a shift register. During the first two cycles of a conversion, the D/A converter is reset to midrange and the analog input is acquired by the sample-and-hold circuit. The S&H then holds this new analog value for the remainder of the conversion period.

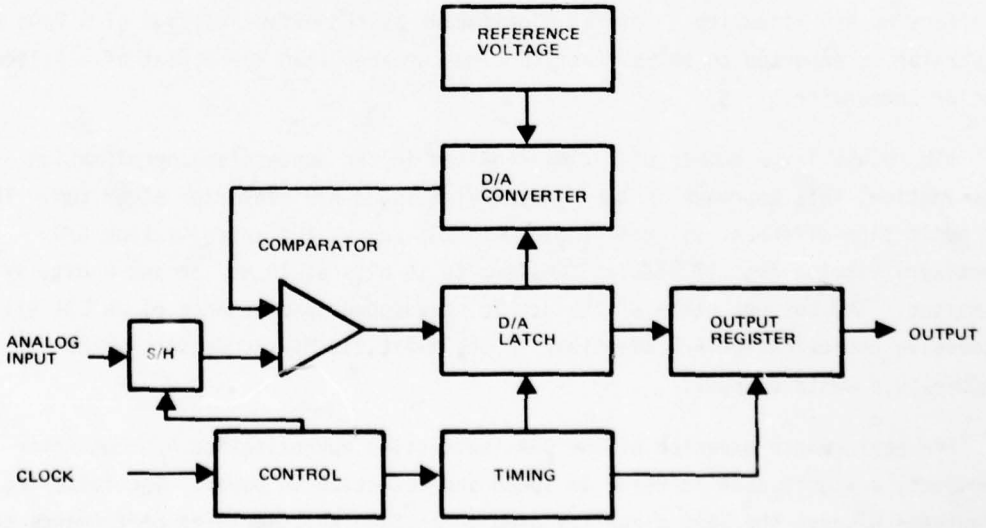



Figure 13. GaAs Successive Approximation A/D

During the third cycle, the comparator compares the held analog signal with the D/A output. The digital result of this comparison is the MSB of the digital output. In the fourth cycle, the D/A converter MSB is set to the value determined in cycle three and the D/A 2SB is turned on. The result of the comparator decision in cycle four is the 2SB of the digital output. The remaining bits are determined in a similar manner, with the analog negative feedback loop, consisting of the D/A converter and comparator, forcing the analog output of the D/A to become a successively closer approximation to the analog input as the conversion progresses. At the end of the conversion, this approximation will be within 1/2 of an LSB of the input, and the digital result of the conversion will be equal to the input to the D/A converter. A final cycle is required to transfer the digital output to a register where it is stored until the end of the next conversion period. The total number of cycles (14) required in the conversion period is two more than the number of bits (12) of A/D accuracy.

The performance of the successive approximation A/D converter is determined by the characteristics of the comparator and the D/A converter. The minimum conversion time of the A/D equals the product of the number of cycles and the cycle time, which is dominated by the D/A settling time and the comparator delay time. The linearity of the A/D converter is determined by the resolution of the comparator, and the linearity of the D/A converter and sample-and-hold circuit.

Successive approximation is the simplest (least complex, low parts count) and most accurate high speed A/D converter algorithm. It is important to note that because only one comparator is used in the design, the comparator offset voltage has no effect on A/D linearity. This is significant as the offset voltage of a GaAs FET comparator is expected to be at least 10 times greater than the offset of a silicon bipolar comparator.

Due to the large number of cycles required in the successive approximation organization, this approach is the slowest high speed A/D converter algorithm. TRW has built five different silicon single chip LSI successive approximation A/D quantizers ranging from 12 bits at 2 Ms/sec to 10 bits at 10 Ms/sec and 8 bits at 15 Ms/sec. The current state of the art in speed/power performance of an LSI silicon successive approximation A/D quantizer is the 8-bit, 15 Ms/sec design, which consumes 0.8 watts of power.

The performance expected of the GaAs successive approximation A/D converter represents a significant increase in speed and reduction in power. The following paragraphs discuss the GaAs circuitry used to achieve this improved performance over conventional silicon LSI techniques.

Comparator

Figure 14 is a circuit diagram of the proposed GaAs FET comparator. The comparator has two modes of operation, track and hold. During the tracking mode, the output follows the input with a small gain. Source followers Q1 and Q2 are used to provide common mode level shifting to the differential common source gain stage consisting of Q3 and Q4. Common gate FET's Q7-10 are used to reduce the Miller effect capacitance within the comparator and to isolate the capacitance of Q3-6 from the load resistors. Large devices (40 μm width) are used for Q3-6. In the tracking mode, Q11 is turned on and Q12 is off. To switch the comparator from track to hold, the control signal at the clock input is changed from a logic "1" to a "0". This turns Q12 on and Q11 off. The comparator gain is consequently increased to near infinity by the positive feedback applied to Q5 and Q6. The small differential analog signal existing at the drains of Q9 and Q10 at the time of the track-to-hold transition is thus amplified to a logic level, resulting in a comparator decision and a usable output.

The speed of the comparator is determined by the magnitude of the time constant associated with the 1.5K load resistors. Each resistor sees the gate-to-drain capacitance of one 5 μm and two 10 μm FET's at 1.5 ff/5 μm and an estimated 3 mils

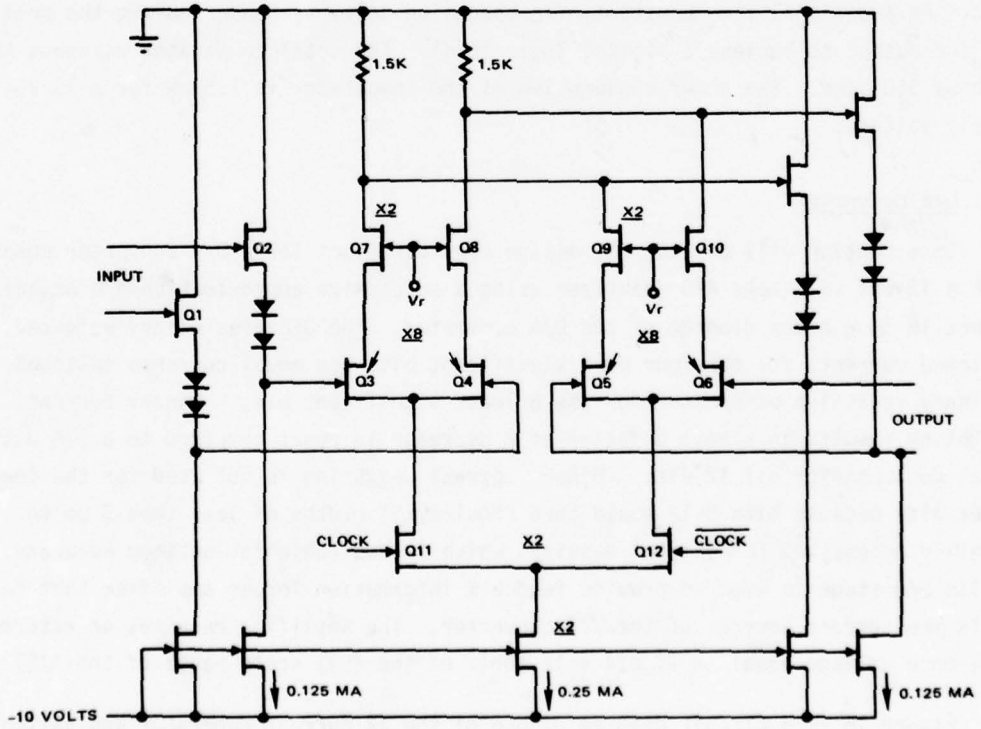



Figure 14. Comparator

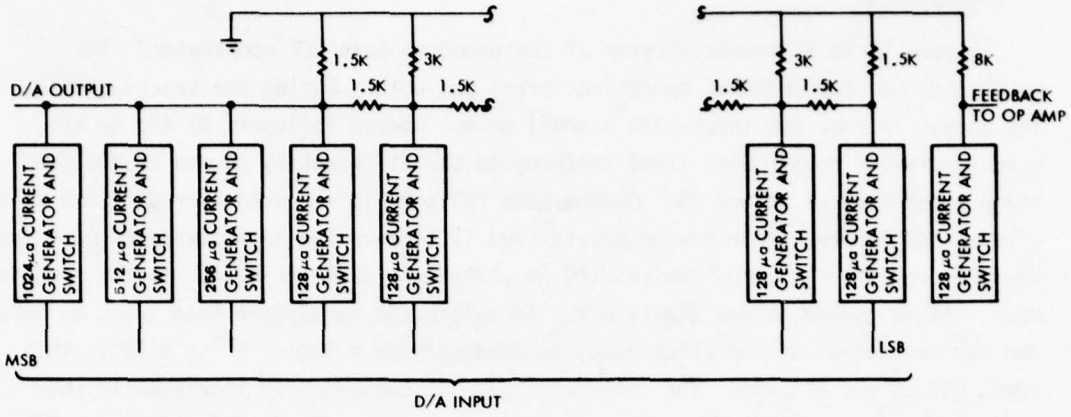



Figure 15. D/A Converter

of interconnect capacitance at 1.6 ff/mil plus device substrate capacitance for a total of 23.5 ff. The time constant is thus 35 psec. The voltage swing across the 1.5K resistor is 375 mV. During the tracking mode, each resistor voltage must change by about 188 mV and settle to within 0.14 mV to result in a 0.1 LSB error referred to the input. The comparator acquisition time thus requires nine time constants or 315 psec. An additional time constant of propagation delay is needed during the hold mode for the output to achieve a digital logic level. The total comparator response time is thus 350 psec. The power consumption of the comparator is 7.5 mW for a 10 volt supply voltage.

D/A Converter

This section will discuss the design considerations for a D/A converter compatible with a 12-bit LSI, GaAs A/D quantizer using a successive approximation A/D organization. Figure 15 is a block diagram of the D/A converter. The D/A uses binary weighted, switched currents for the four most significant bits and equal currents switched into a binary resistive attenuator for the 8 least significant bits. Binary current weighting results in almost a factor of 2 decrease in power compared to a D/A using equal currents for all 12 bits. Binary current weighting is not used for the lower order bits because bits 5-12 would then require FET widths of less than 5 μm to maintain a constant FET current density, which is desirable for optimum accuracy. A 13th D/A stage is used to provide feedback information for an amplifier that controls the current sources of the D/A converter. The amplifier requires an external reference voltage equal to -1.024 volt (half of the full scale range of the A/D).

Figure 16 is a circuit diagram of one of the 12 current generator and switch sections of the D/A converter. The current source is biased with a thin film

resistor, which can be laser trimmed to adjust the output of the current source. The nominal voltage drop across the thin film resistor is 4 volts. The 25 mV threshold uncertainty of the current source FET thus results in a 0.6% uncertainty in the current source output, which is corrected by laser trimming. The untrimmed current source accuracy could be increased at the expense of power consumption by increasing the voltage across the resistor. Laser trimming of the resistor would still be necessary. Reducing the resistor voltage would result in a need for increased laser trimming, which would begin to significantly change the temperature coefficient of the trimmed resistor and thus reduce the useful temperature range of the A/D converter.

The current switch consists of a differential pair of depletion mode FET's. The switch is turned on by applying a logic "1" to the gate of Q2 and a logic "0" to the gate of Q1. This allows the output of the current source to pass through Q2 to the D/A load resistor. When Q1 is turned on, the current is discarded to ground. The use of depletion mode devices ensures that gate current is zero.

The settling time of the D/A converter is determined by the time constant at the output of the D/A: $\tau = RC$, where R is the D/A output impedance and C is the total capacitance of the D/A current switches and the comparator input. For a 5 μm depletion FET, Idss = 125 μA, and Cgd = 1.5 ff. For a thin film resistor at 1000 ohms per square, C = 0.28 ff/mil$^2$ (parallel plate) + 1.27 ff/mil (fringing effects) for a total of 1.6

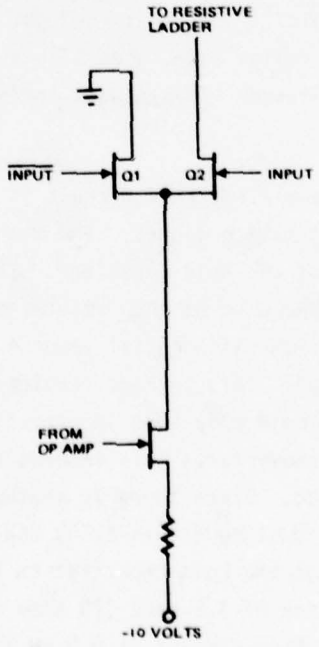



Figure 16. Current Generator and Switch

ff/KΩ. The capacitance of the comparator input source follower is 1.5 ff and the capacitance of the estimated 5 mil length of interconnect is 8 ff.

Thus,

$$\tau = RC$$
$$\tau = 1K\ (16\ Cgd + 15\ C_{D\text{-}sub} + C_R + C_I)$$
$$\tau = 1K\ (16\ (1.5) + 15\ (2.0) + 1.6 + 8.0)$$
$$\tau = 1K\ (24.0 + 30.0 + 1.6 + 8.0)$$
$$\tau = 1K\ (64)$$
$$\tau = 64\ \text{psec}$$

Nine time constants are required for D/A settling in a 12 bit successive approximation A/D. Total D/A settling time is thus 576 psec. Power consumption of the D/A is 28.8 mW using a 10 volt supply voltage.

Sample and Hold

When an A/D converter is used to convert a wide bandwidth analog signal, a sample and hold circuit is needed to sample the analog signal and hold the sampled analog voltage constant for the conversion time of the quantizer. A circuit diagram of a monolithic GaAs sample and hold is shown in Figure 17. Source follower Q1 is a preamplifier, which drives a Schottky, diode bridge switch consisting of D1-4. The output of the diode switch drives a hold capacitor. The hold capacitor voltage is buffered by the source follower postamplifier, Q2. Transistors Q3 and Q4 control the diode switch. When S is a logic "1", Q4 is turned on, the switch is conducting and the sample and hold is in the follow mode. When S is a logic "0", Q3 is turned on and the diode switch is reversed biased. This causes the sample and hold to be in the hold mode.

The performance of the sample and hold circuit is largely dependent on the reverse leakage current of the switch diodes. The magnitude of this leakage determines the required size of the hold capacitor. The time constant of the hold capacitor and the output impedance of Q1 then determines the acquisition time of the sample and hold. The maximum differential reverse biased leakage of diodes D2 and D4 is estimated to be 50 pA. This leakage requires a hold capacitor of 5 ff to obtain a voltage drift in the hold mode that is compatible with a 12 bit, 50 Ms/sec successive approximation A/D converter. This ensures that the drive is adequate for rates of 25 Ms/sec to 70 Ms/sec. Since there is another 10 ff of transistor and interconnect capacitance that must be driven by Q1 and the output impedance of Q1 is about 10K, the time constant of the hold capacitor is 150 psec. This results in a sample and hold acquisition time of 1.5 nsec (10 time constants). The power consumption of the sample and hold circuit is 5.0 mW for a 10 volt supply voltage.

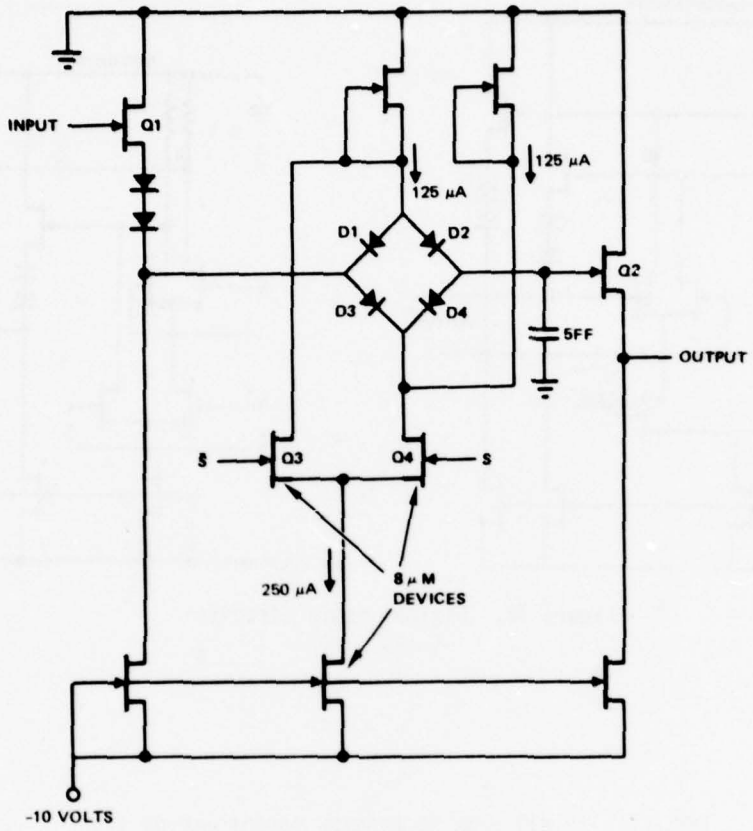



Figure 17. Simplified Sample and Hold Circuit

Digital Logic Circuits

An A/D converter requires digital logic circuitry for its timing, control, and output data formatting functions. Two basic types of logic circuits are needed: a gate and a latch. Circuit diagrams of these circuits are shown in Figure 18. The differential circuit configuration reduces noise currents, which is an advantage in a high resolution A/D converter. The power consumption of this logic circuitry is 0.36 mW per gate or latch. The propagation delay is 0.1 nsec.

Successive Approximation A/D Performance

The speed and power consumption of the A/D converter can be calculated now that the circuitry has been defined. The complete conversion period for a 12-bit successive approximation A/D converter requires 14 separate cycles. The minimum length of each cycle is equal to the sum of comparator response time 350 psec, D/A delay plus settling time 640 psec, and latch propagation delay 100 psec. Total cycle time is 1.09 nsec and the minimum conversion period is 15.3 nsec. This is

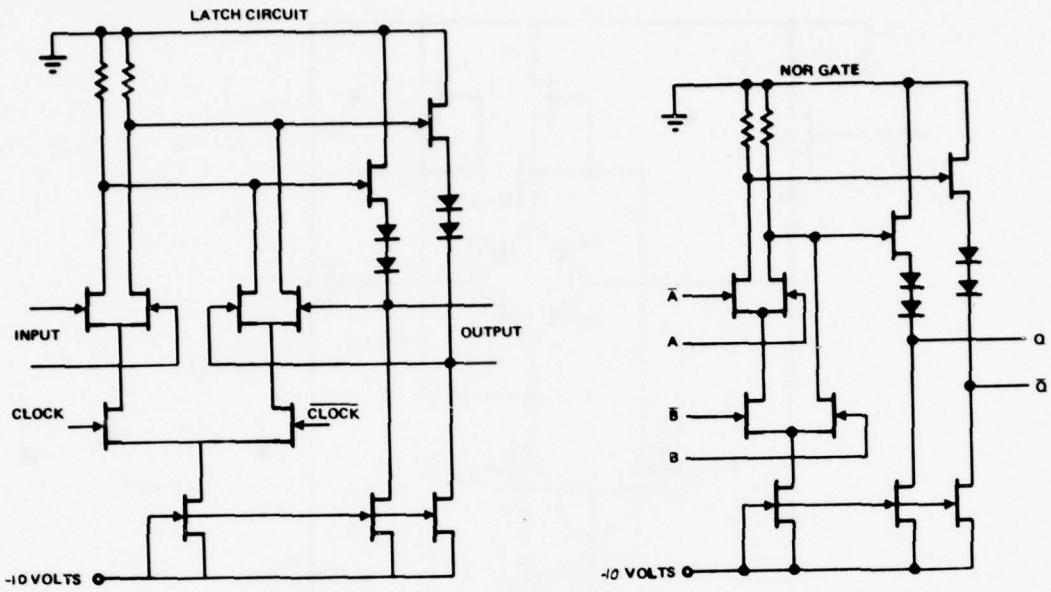



Figure 18. Digital Logic Circuits

TABLE I 12 BIT GaAs SUCCESSIVE APPROXIMATION A/D TIMING BUDGET

| | |
|---|---|
| COMPARATOR DELAY | 35 PSEC |
| LATCH DELAY | 100 PSEC |
| D/A DELAY + SETTLING | 640 PSEC |
| COMPARATOR ACQUISITION TIME | 315 PSEC |
| TOTAL TIME PER CYCLE | 1090 PSEC |
| CONVERSION PERIOD (14 CYCLES) | 15.3 NSEC |
| CONVERSION RATE | 65.5 MSPS |

equivalent to a 65.5 Ms/sec conversion rate as shown in Table I.

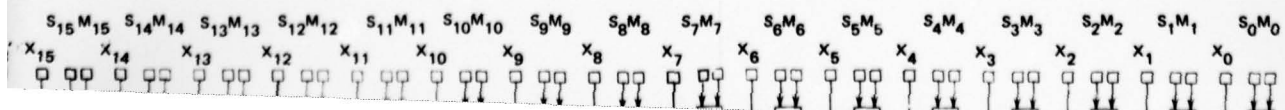
Total A/D power consumption is equal to the sum of the power required by the sample and hold circuit (5.0 mW), comparator (7.5 mW), D/A converter (28.8 mW), digital logic circuitry (39.6 mW), and the output buffers. Assuming the desired output interface is an ECL differential 400 mV signal with a 4 nsec risetime driving a 10 pF load, the output buffers require 60 mW. Total A/D converter power consumption is 140.9 mW, with nearly half of the total power used in the output buffers, as shown in Table II. The required power supply voltage is -10V.

The analog input range of the A/D is 0 to -2.048 V. An input clock signal is required. The frequency of this clock should be 14 times the conversion rate (700 MHz at 50 Ms/sec). The digital output is provided in a parallel format. Approximately 800 devices would be required to construct the successive approximation A/D. This would result in a chip size of about 60 mils x 80 mils.

TABLE II 12 BIT GaAs SUCCESSIVE APPROXIMATION A/D POWER BUDGET

| CIRCUIT | POWER (MW) |
|---|---|
| SAMPLE AND HOLD | 5.0 |
| COMPARATOR | 7.5 |
| D/A LATCH REGISTER | 14.4 |
| D/A CONVERTER | 28.8 |
| TIMING AND CONTROL | 16.8 |
| OUTPUT REGISTER | 8.4 |
| OUTPUT DRIVERS | 60.0 |
| TOTAL POWER | 140.9 |





Feed Forward A/D Converter

Figure 19 is a block diagram of a 10-bit LSI GaAs feed forward A/D converter. The A/D consists of two stages, each containing a 5-bit quantizer (31 comparators and combining logic). The output of the first 5BQ drives a D/A converter, which is used to modify the reference input of the second stage 5BQ. The comparator threshold voltages of the second 5BQ are 32 times closer together than those of the first 5BQ. This provides the increased resolution needed to determine the 5 least significant bits of the 10-bit digital output. The outputs of both 5BQ's are stored in a latch for parallel output or scanned by a multiplexer to provide a 10-bit serial output.

Because only two cycles are needed in the feed forward A/D converter, this A/D has a significantly faster conversion rate than the successive approximation A/D discussed in the previous section. However, the feed forward organization requires considerably more laser trimming than the successive approximation A/D. In addition to the D/A converter each of the 62 comparators must be trimmed. This results in an accurate A/D at some nominal temperature, but accuracy will degrade over temperature more than in the successive approximation A/D converter.

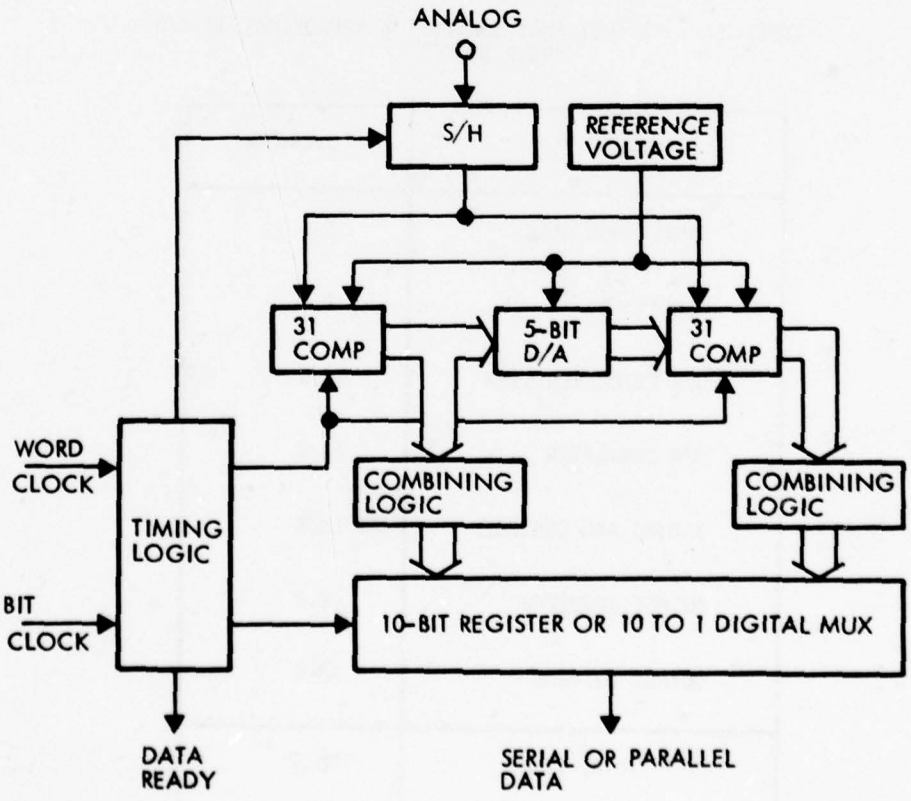



Figure 19. Feed Forward A/D Converter

## Feed Forward A/D Circuitry

The circuitry used in the feed forward A/D converter is similar to that already discussed for the successive approximation A/D converter. The major difference is caused by the higher load capacitance of the multiple conparators used in the feed forward A/D. The sample and hold circuit must drive 62 comparator inputs at 1.5 ff per comparator and approximately 100 mils of interconnect at 2 ff per mil for a total of 293 ff. A two-stage postamplifier is required to drive this capacitance with a 100 μm FET used as the output source follower. This results in a 400 ohm output impedance for the sample and hold and a 117 psec time constant. The settling time at the sample and hold output is thus 1.17 nsec (10 time constants). The power consumption of this sample and hold is 9.6 mW. A linear D/A converter is used in the feed forward A/D converter. The D/A consists of 31 current generator and switch circuits driving a single load resistor.

Each D/A stage is driven by one of the 31 comparators in the first stage 5BQ. This arrangement allows the D/A converter to begin settling before the combining logic has decoded the 5BQ output. The 31 D/A output transistors are 10 μm FET's with a total combined capacitance of 93 ff. The capacitance of the 31 comparator inputs of the second stage 5BQ is 47 ff, and the estimated interconnect capacitance is 200 ff. The total capacitance driven by the D/A is thus 340 ff. Each D/A switch current is 125 μA, which requires a 256 ohm load resistor for a 1.024 volt full scale analog range. The D/A time constant is thus 87 psec, and the D/A settling time is 870 psec (10 time constants). Power consumption of the D/A converter is 19.2 mW.

## Feed Forward A/D Performance

The minimum conversion time of the feed forward A/D converter is equal to the sum of sample and hold acquisition time (1.5 nsec), sample and hold settling time (1.17 nsec), comparator response time in the first 5BQ (.68 nsec), D/A settling time (.84 nsec), and comparator response time in the second 5BQ (.68 nsec). The total conversion time is thus 4.90 nsec, which is equivalent to a conversion rate of 204 Ms/sec.

Power consumption of the feed forward A/D is equal to 300 mW. Approximately half of the total power is consumed by the output buffer circuits. A total of 3000 devices are used in the feed forward A/D for an estimated chip size of 110 mils on a side.

## Conclusions

The A/D converter organization that best meets any requirement is dependent on the performance goals. A comparison of the performance of the successive approximation

and feed forward converters is shown on Table III.

Table III A/D Converter Comparison

| PARAMETER | SUCCESSIVE APPX. | FEED/FORWARD |
|---|---|---|
| Number of bits | 12 | 10 |
| Speed (megasamples/second) | 50 | 200 |
| Clock rate (megahertz) | 700 | 400 |
| Power (milliwatts) | 150 | 300 |
| Temperature range | wide | more restricted |
| Number of devices | 800 | 3000 |
| Chip size (mils) | 60 x 80 | 110 x 110 |
| Manufacturability (cost) | good | more difficult |

## A.3 16 X 16 MULTIPLIER

A high speed multiplier is essential in any advanced signal processing systems where realtime operation is required. Typical applications are found in digital filters, fast Fourier transform processors, computer circuits, or other special digital signal processors. Tranditionally, multiplication has been a time-consuming operation requiring rather complicated circuitry and a large amount of power. This difficulty is especially severe in the systems where many repeated multiplications are required to complete an operation. To circumvent this limitation, TRW developed a series of high performance MSI and LSI multiplier circuits* in the past 10 years. The most recent 16 x 16 multiplier MPY-16H) uses gates with delay-power products of less than 0.2 pj and completes the multiplication cycle in 100 nsec. Presently available data on GaAs FET's indicates that the performance of the multiplier is expected to improve at least by two orders of magnitude if GaAs gates are used instead. This section discusses optimum 16 x 16 multiplier configurations for low power, high speed performance and circuit descriptions and techniques for achieving a multiplication rate of 100 MHz.

### 16 x 16 Multiplier Configuration Tradeoffs

A number of multiplier concepts have been studied at TRW that can potentially achieve 16 x 16 multiplication rates in the range of 50 to 150 MHz with low power dissipation.

Although hard conclusions have not been made at this time, and overall studies should be concluded in parallel with device and process development, basic multiplication building block requirements and desirable device characteristics can be identified now. The approaches studied include:

- All-parallel
- Serial-parallel
- Byte serial-parallel
- All-serial.

The value of these preliminary studies is that they permit detail concept tradeoffs based on present and projected GaAs device performance, achievements, complexity, producibility, power, reliability, and cost.

### All-Parallel 16 x 16 Multiplier Concept

The all-parallel multiplier accepts both parallel multiplicand and parallel multiplier words at the same time. Upon completion of multiplication, the results are also available in parallel format. The multiplier multiplies, shifts, and adds

*G McIver, et al "A Monolithic 16 x 16 Multiplier," ISSCC, Feb 74, p. 54, and U.S. Patent 3,900,724.

the partial products simultaneously. Since all operations are performed in parallel, the all-parallel multiplier is the fastest multiplication technique. It can meet the speed requirement of a 100 MHz word multiplication rate. One of the significant advantages of this approach is that the speed requirements of all the basic cells in the multiplier are uniform. Therefore for the same multiplication word rate, the demanded speed requirements of the basic cell is the least, compared with the serial-parallel and all-serial approaches with the same power constraint. The all-parallel approach is obviously the most promising approach for the demonstration of a 16 x 16 multiplier in terms of speed.

Serial-Parallel 16 x 16 Multiplier Concept

The serial-parallel multiplier loads the multiplicand word in parallel but the multiplier word is entered serially. The multiplication is performed between the multiplicand word and the multiplier bit starting with the LSB. At the completion of each bit-word multiplication, the result is shifted right one position and made ready for the next higher-order bit multiplication. The process continues until all multiplier bits are used. The final result is shifted out serially. This approach is good for low speed applications, since, by performing the multiplication serially, some complexity and power reductions are realized. This, in turn, reduces the chip size requirement and eventually enhances the fabrication yield. However, if the minimum word multiplication rate is 100 MHz, the bit clock rate has to be 32 times higher or 3.2. GHz. Since the basic GaAs FET logic gate is designed for low power as well as high speed operation, requiring the gates to operate over a wide frequency range (more than one order of magnitude) on the same chip is obviously not optimum.

Byte-Serial-Parallel 16 x 16 Concept

This is a hybrid approach between the all-parallel approach and serial-parallel approach. The multiplicand word is loaded in parallel but the multiplier word is loaded in bytes of 4 bits. The multiplication is performed in groups of 4-bit bytes. If the multiplier is designed according to this approach, some savings in complexity can be realized without the penalty of having to operate the logic gate over a wide frequency range. However, more control logic circuits are required to sequence the operation of the multiplier than the all-parallel approach. Some external circuits are also required to group the multiplier into 4-bit bytes.

All-Serial 16 x 16 Concept

In this approach, a single multiplication cell performs all the bit-by-bit multiplications, partial product summing, and shifting. A clock as high as 16 x 16 = 256 times the word multiplication rate is required. If the word multiplication is set at

100 MHz, then a 25.6 GHz logic family is needed. A GaAs transferred electron device (TED) can theoretically be designed to handle the data rate but not at the allowable power. Furthermore, interfaces with other system functions (at serial data rates of 25 GHz) would be a significant problem.

Since GaAs TED's suffers another serious drawback of being unsuitable for analog circuits, the all-serial multiplier is not practical for this effort.

Summary and Conclusion of the Configuration Tradeoffs

The key parameters of the four multiplier configurations are summarized in Table 1 for comparison. The choice of the recommended 16 x 16 multiplier organization concept must be based on a number of considerations, most of which are key to the achievement of high speed, low-power arithmetic function in an LSI implementation. The significant considerations of this choice are:

- Multiplication word rate of 100 MHz/sec
- Total power dissipation of less than 100 mW
- The GaAs devices used are also usable in low-power wideband analog circuits
- Complexity
- Packaging and interconnects
- Technical risk.

Table 1. Organization Concepts Summary

| Organization | Power | Speed | Requiring External Circuits | Circuit/ Device Development | Frequency of Interface Signals |
|---|---|---|---|---|---|
| All-parallel | Moderate | High | No | Simple | Low |
| Serial-parallel | Low | Low | Yes | Moderate | High |
| Byte-serial-parallel | Moderate | Moderate | Yes | Moderate | Moderate |
| All-serial | High | Low | Yes | Extensive | Very high |

The all-serial multiplier using TED devices is not recommended because the TED devices operate very inefficiently at the frequencies of interest here. Furthermore, the TED devices developed would have very little chance of being used in the analog circuits.

The serial-parallel approach requires some of the circuits to operate at a 3.2 Gbps rate. To achieve this, the gate delay would have to be less than 0.1 nsec, which involves technical risks that are sufficient to made the serial-parallel approach unattractive.

The byte-serial-parallel approach requires some additional external circuits to regroup the input words to a usable format. It is a clumsy approach from a user standpoint.

The all-parallel concept offers the following distinct advantages:

- Highest word rate/power ratio, (i.e., high processing speed per unit power)
- No critical high frequency interfaces
- No extra external circuits required
- The similar GaAs FET device can also be used in low-power analog circuits.

TRW has experience in building both all-parallel and serial-parallel multipliers for different applications using the same devices. The (word rate)/power ratio of the all-parallel approach is 42 percent better than the serial-parallel approach. Since both speed and power are very important in future advanced signal processing systems, the 16 x 16 multiplier organization recommended is the all-parallel approach.

Multiplier Design

All-Parallel Multiplication Algorithms

Several basic parallel multiplication algorithms have been considered for realization of a low power, high speed digital multiplier. Some algorithms require pipeline latches and some do not. In general, the speed requirement of the basic cells in pipelined multipliers is only a small fraction of that of the nonpipelined ones, depending on the algorithms used. As a result, a big saving in power and a sizable reduction in speed-power products of the logic gates can be realized. However, pipelined multipliers have very limited usage in modern systems due to their intolerable long throughput delays. Therefore, pipelined multipliers, despite their superficially good speed-power product and low power, are not recommended.

In selecting an algorithm for implementation, the following criteria are of importance:

- Representation of negative numbers
- Basic algorithm (e.g., carry save, Booth, Wallace, Dadda).

Negative Number Representation. Three basic systems have been widely used for binary number representation of negative numbers: sign-magnitude, 1's complement, and 2's complement. Although each has certain advantages, the 1's complement system seems least desirable for an arithmetic element such as the very high speed multiplier. The sign-magnitude representation yields the simplest possible multiplier structure, as all multiplications are performed using the magnitude with the product sign determined from the operand signs. The 2's complement system requires that correction terms be considered in computing the product if either (or both) of the operands is negative. Thus, superficially it would seem desirable to use the sign-magnitude system. A complication arises, however, if significant addition (or subtraction) is performed, with the results of the multiplication as the case with fast Fourier transform (FFT) processors, since addition or subtraction is considerably simpler with 2's complement numbers.

A final consideration is that although a 2's complement multiplier can multiply sign-magnitude numbers (by hardwiring the sign bits of the operands to indicate that both operands are positive and determining the product sign separately), the opposite is not true. Thus, upon considering the probable need for subsequent addition and the desirability of being able to perform either 2's complement and sign-magnitude multiplication in the same multiplier, the 2's complement negative number representation is proposed.

In selecting the basic algorithm, many options are available, including Booth's algorithm,[1] the Wallace multiplier,[2] Dadda's scheme,[3,4] the carry-save approach,[5] and the Pezaris adder array.[6]

Basic Algorithm. Even though many multiplication algorithms have been developed over the past 30 years, the requirement of 2's complement representation for negative numbers and 10 nsec throughput delay narrows the number of choices to two algorithms:

- Dadda's scheme
- Sequential-add[7] (a nonpipelined Booth's method).

Each is described below.

Dadda's scheme[3,4] and its predecessor Wallace's method[2] involve forming the bit product matrix and then using full adders to reduce the matrix to a two-row matrix

(i.e., to two binary numbers). The rows of the two-row matrix are then added in a fast adder (e.g., a carry look-ahead adder) to give the desired product. As shown in Dadda's first paper,[3] the reduction of the bit product matrix to an equivalent two-row matrix takes six adder delays for a 16 x 16 multiplier. A potential drawback exists in that Dadda's scheme was developed for sign-magnitude numbers. Recently[8] this problem has been overcome by adding correction terms to the partial product matrix. In some cases, inclusion of the correction terms may add one adder delay to the reduction time for the bit product matrix.

The main disadvantage of this method is that of implementation complexity. In terms of implementation the formation and reduction of the bit product matrix is performed with one integrated circuit type (consisting of full adders and gates), while the 32-bit addition is performed with a second integrated circuit type (consisting of carry look-ahead adder blocks). This dual-integrated circuit development is seen as a major drawback to this approach.

The second algorithm, sequential-add, computes asynchronously and can be used with either 2's complement or sign-magnitude binary number notation.

If two numbers in sign magnitude notation

$$X = X_{M-1}2^{M-1} \cdot \cdot \cdot + X_2 2^2 + X_1 2^1 + X_0 2^0$$

$$Y = Y_{N-1}2^{N-1} \cdot \cdot \cdot + Y_2 2^2 + Y_1 2^1 + Y_0 2^0$$

are to be multiplied, the product is

$$P_{i+j} = \sum_{i=0}^{M-1} \sum_{j=0}^{N-1} X_i Y_j 2^{i+j}$$

The sequential-add approach forms all of the partial products simultaneously. Equally weighted partial product-sum terms are added together with equally weighted carry terms from the next lower partial products. Thus

$$P_0 = X_0 Y_0$$

$$P_1 = (X_1 Y_0 + X_0 Y_1) + (C_{X_0 Y_0}),$$

$$P_2 = (X_2 Y_0 + X_1 Y_1 + X_0 Y_2) + (C_{X_0 Y_1} + C_{X_1 Y_0})$$

.

.

etc., for all output product-terms (Note: $C_{X_iY_j}$ means the carry term resulting from the partial product of $X_i$ and $Y_j$, etc.).

Multiplication of 2's complement binary numbers is performed by adding correction terms which become zero for the sign-magnitude case. The magnitude of the product, in both systems of notation, can be shown to be the summation

$$P = (XY) + (Y_S\overline{X}) + (S_S\overline{Y}) + (X_S + Y_S) \qquad (2\text{-}1)$$

where

P = magnitude of the product

X and Y = magnitude of the multiplier and multiplicand

$X_S$ and $Y_S$ = sign of the multiplier and multiplicand; zero for positive numbers

The sign of the product is formed separately by an exclusive-OR circuit in both systems of notation, such that

$$P_S = (X_S) \oplus (Y_S)$$

where

$P_S$ = sign of the product.

Both $X_S$ and $Y_S$ are assumed zero in equation (2-1) when sign-magnitude numbers are multiplied. In this case, the equation reduces to

$$P = XY$$

The following example illustrates how the multiplier computes 2's complement numbers:

Example:

If both $X_SX$ and $Y_SY$ are negative numbers, then

$$P = (XY) + Y_S\overline{X} + (X_S\overline{Y}) + (X_S + Y_S)$$

Take

$(X_SX)$ = (1) 0 1 0 1 (= -11 in decimal notation)

$(Y_SY)$ = (1) 0 0 1 1 (= -13 in decimal notation)

$(P_SP)$ = (0) 1 0 0 0 1 1 1 1 (= +143 in decimal notation)

consumption of the sample and hold circuit is 5.0 mW for a 10 volt supply voltage.



```
          0 1 0 1
          0 0 1 1
        ---------
          0 1 0 1
        0 1 0 1
      0 0 0 0
    0 0 0 0
  ---------------
  0 0 0 0 1 1 1 1   (XY)
  1 0 1 0           (Y_S X)
  1 1 0 0           (X_S Ȳ)
        1           X_S
        1           Y_S
  ---------------
P = 1 0 0 0 1 1 1 1 (which is correct)
```

Of the two algorithms described above, the sequential-add is obviously the better compromise. It requires the development of only one integrated circuit type and can be used with either sign magnitude of 2's complement binary notation. Therefore, the sequential-add algorithm is recommended for the 16 x 16 multiplier.

Sequential-Add Multiplier Design

The basic sequential-add multiplier utilizes the iterative building block shown in Figure 20 at each computational node. The $X_i$ $Y_j$ partial product terms are generated by AND gates. These partial products are added to the vertically transferred sum and diagonally transferred carry terms for adjacent computational nodes.

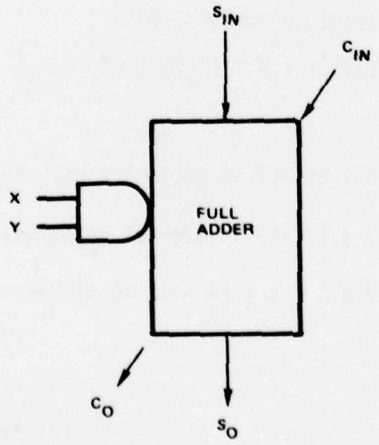



Figure 20. Sequential-Add Iterative Building Block

delay plus settling time 640 psec, and latch propagation delay 100 psec. Total cycle time is 1.09 nsec and the minimum conversion period is 15.3 nsec. This is



Figure 21 shows the complete logic diagram of the 16 x 16 multiplier. It can be seen from inspection that the magnitude of the product ($C_o$, $P_{31}$, $P_{30}$ · · · $P_1$, $P_0$) is the sum of the terms given in equation (2-1). When the circuit is used as a single 16 x 16 multiplier, $Y_s'$ is connected to $Y_s$, and $X_s'$ to $X_s$. Also, all S and M terms are unused and therefore connected to logic "0". The sign bit is formed separately by the exclusive-OR circuit. The 16 x 16 multiplier is expandable into larger computational arrays of 16N x 16M, where N and M are integers greater than one. No additional circuitry is needed except for N x M multipliers.

The outputs $P_0$ through $P_{15}$ are not used. However, they are brought out to pads to facilitate multiplier expansion.

Since only the 16 most significant bits out of 32-bit product words are of interest, an optional round-off circuit can be added to advance the product output one additional count whenever the analog equivalent of the unused 16 less significant bits is more than 1/2 of its maximum magnitude. (This circuit is not shown in Figure 21 for clarity.)

Circuit Description

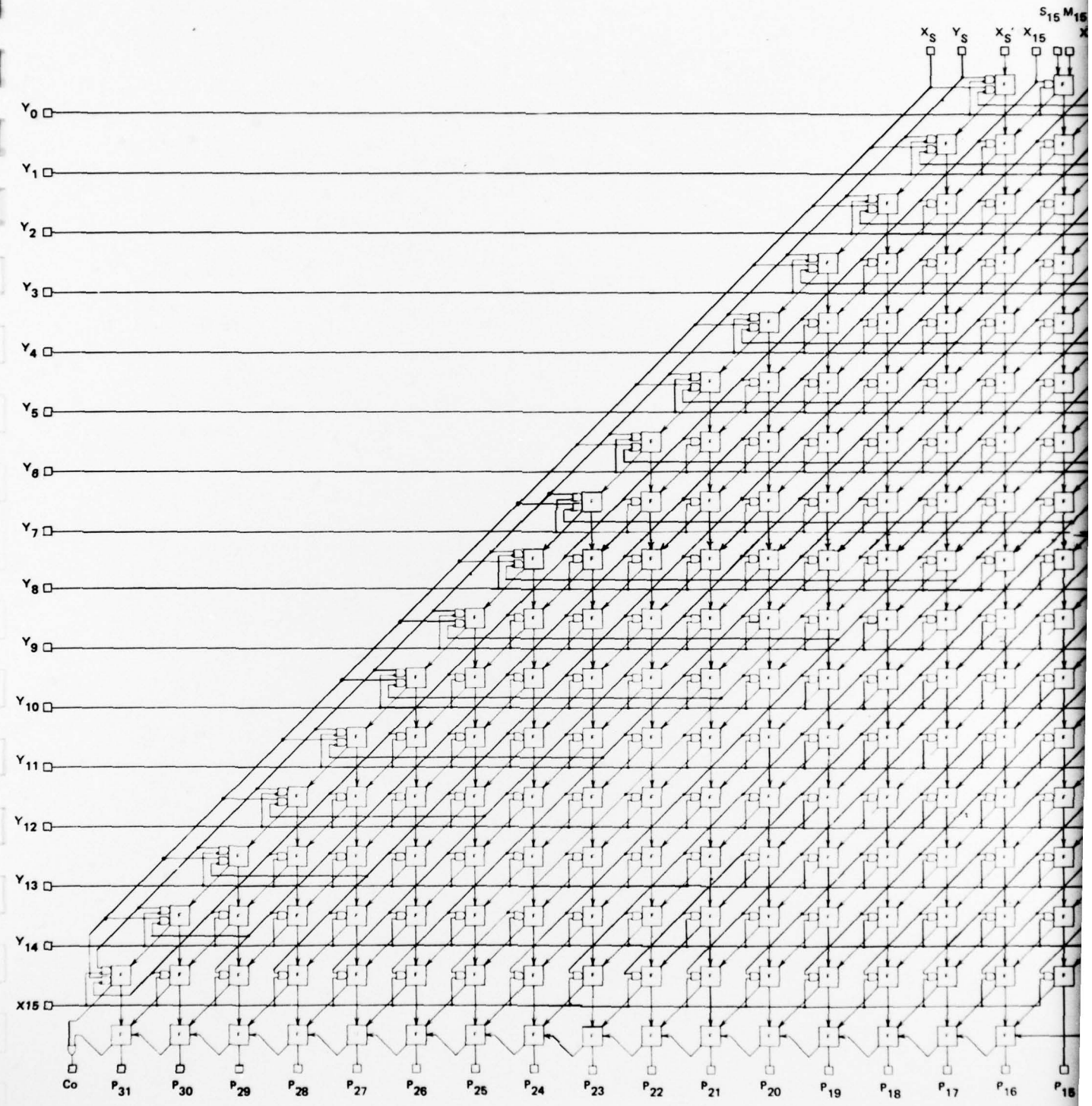
Several different ways of designing low power, high speed digital circuits using GaAs FET's have been investigated. They include Schottky diode logic, saturated logic, and current mode logic. Each of these logic families has its own advantages and disadvantages. The investigation concluded that differential current mode multilevel logic is superior for the multiplier application because:

- It provides the best speed performance for this high speed requirement
- It has high noise immunity
- Both the output and its complement are available, making efficient multiplier cell design possible
- It can easily interface with existing high speed ECL circuits
- It offers high power supply noise rejection and wide temperature range.

Implementation of the differential current mode logic basic cell is shown in Figure 22. This circuit contains nine gates using 39 components (FET's and resistors). Notice that many of the FET's share the same drain. Many others share the same source. These sharings of the drains and sources eliminate the need of many isolation wells and thus reduce the overall cell and chip size. Part of the basic cell circuit that generates $S_o$ was laid out using the APPLICON computer-aided design system. The resulting plot is shown in Figure 23. The total area of the basic cell takes 6 x 8 mils.

| | |
|---|---|
| CONVERSION RATE | 65.5 MSPS |





| | |
|---|---|
| TOTAL POWER | 140.9 |



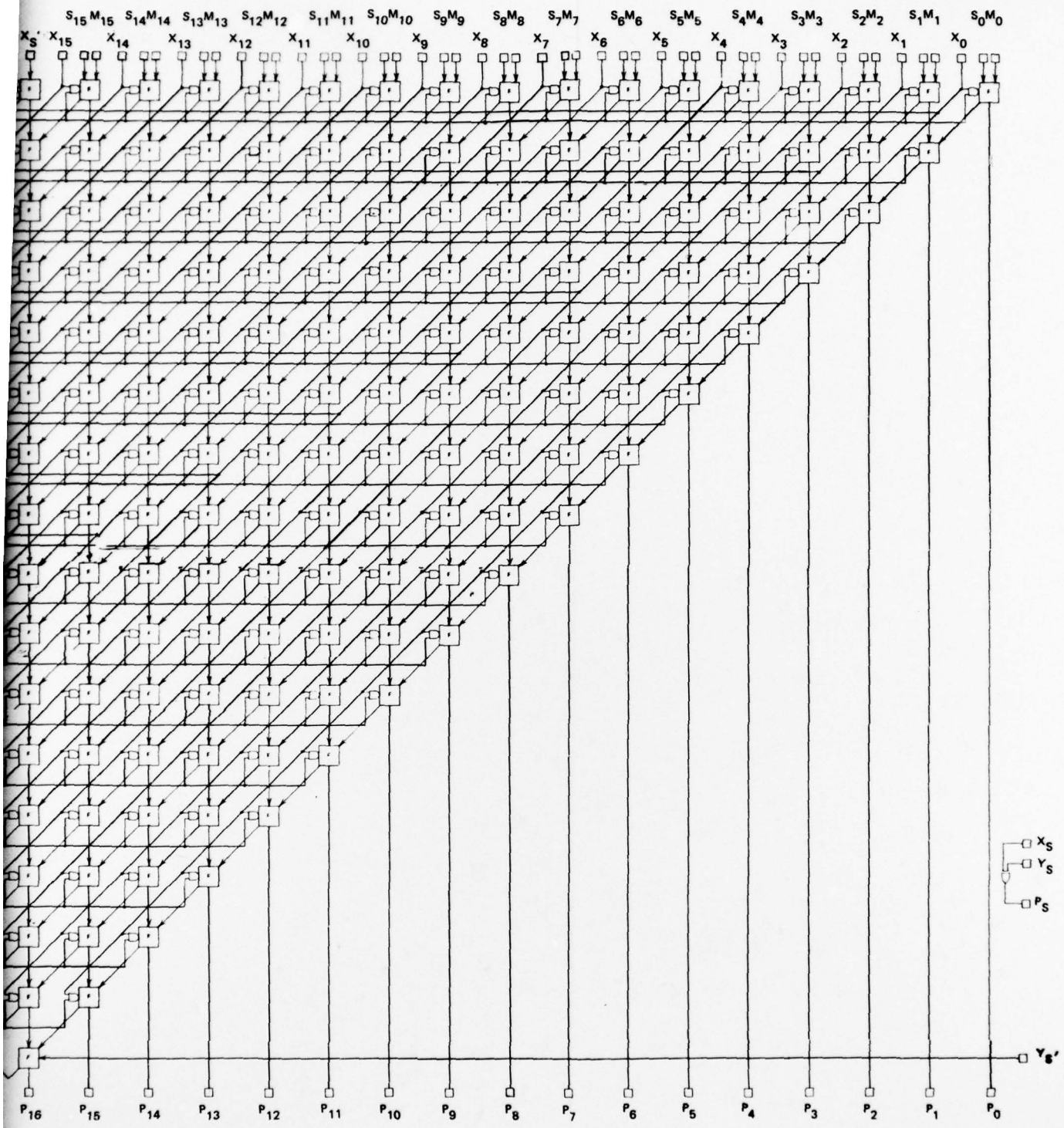



Figure 21. 16 x 16 Multiplier Logic Diagram

DATA READY

SERIAL OR PARALLEL DATA

Figure 19. Feed Forward A/D Converter



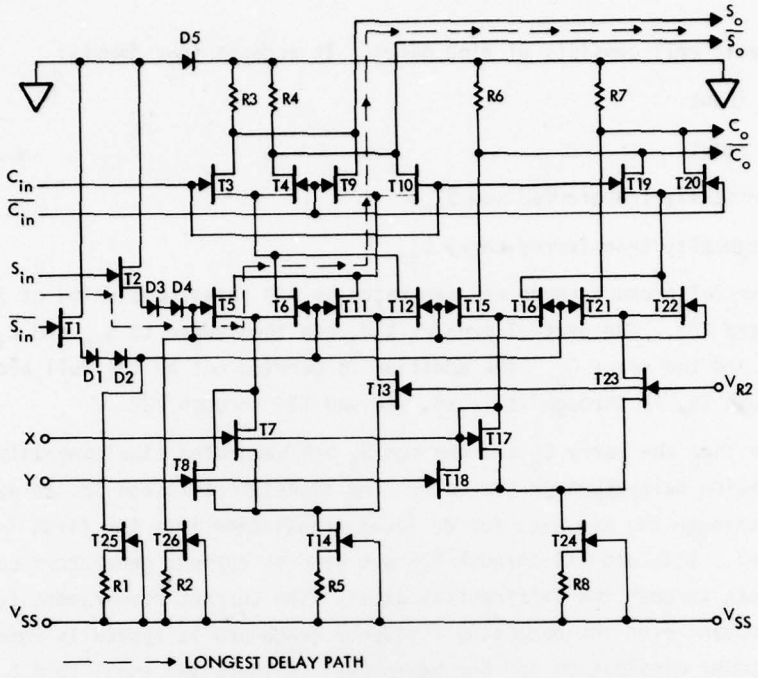



Figure 22. Differential Current Mode Logic Implementation of Basic Cell

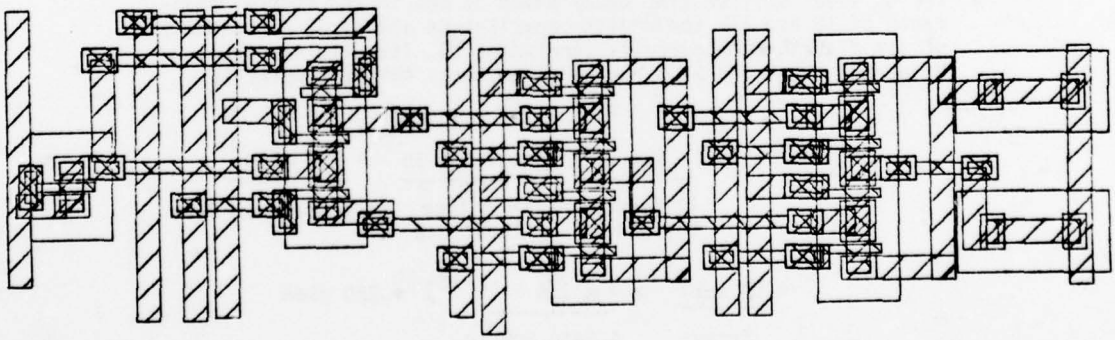


Figure 23. Half-adder Part of the Basic Cell



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The A/D converter organization that best meets any requirement is dependent on the performance goals. A comparison of the performance of the successive approximation



The basic cell consists of nine,gates. It accepts four inputs:

- $X_i$ input
- $Y_j$ input
- Vertically transferred sum $S_{in}$
- Diagonally transferred carry $C_{in}$

The $X_iY_j$ partial product terms are generated by AND gates consisting of T7, T8, T13, T17, T18, and T23. The partial product $X_iY_j$ are then added to $S_{in}$ and $C_{in}$ to generate the sum $S_o$ and the carry $C_o$. The addition is carried out by the full adder consisting of T3 through T6, T9 through T12, T15, T16 and T19 through T22.

Notice that the carry $C_o$ and the sum $S_o$ are generated simultaneously to minimize the propagation delay through the cell. The transistors T1 and T2, as well as the diodes D1 through D4, are used for dc level translation from the first level to the second level. T14, and T24 through T26 are used as current generators controlling the bias currents through the differential gates. The current requirement for basic cell remains constant over the operating frequency range and is typically equal to 128 μA. The total power dissipation for the basic cell is therefore equal to 4.5 volts x 128 μA = 576 μW.

One of the most important performance parameters in the basic multiplier design is the propagation delay or the speed of the arithmetic operations. For this particular differential current mode logic design, the longest path of the operation is shown in dotted lines from $S_{in}$ to $S_o$. The delay time through this longest path can be divided into three parts and calculated as follows:

- The dc level shifter time delay which is due to the source resistance of T2 and all the device capacitances and stray capacitances of its distribution circuits (including T5, T12, T15 and T22). Using the projected X1.5 device parameters, the time delay is

$$t_{d1} = (\ln 2)\ \underbrace{(7.6 \times 10^{3})}_{\text{T2 Source Resistance}}\ [\underbrace{4 \times 3.6 \times 10^{-15}}_{\text{4 Miller Input Cap}} + \underbrace{2.4 \times 10^{-15}}_{\text{T26 Drain-to-Gate}}$$

$$+ \underbrace{10 \times 10^{-15}}_{\text{Stray}} + \underbrace{4 \times 3.6 \times 10^{-15}}_{\text{4 Gate Source Input Cap}}] = 220 \text{ psec}$$

- The source-to-drain propagation delay of T9. This can be found from the GaAs model and is

$$t_{d2} = (\ln 2) \times [4R(0.5) + 3R(1.8) + 2R(1.8) + R(1.8)] \times 10^{-15}$$

Where

R = 1.33K for the X1.5 devices.

Substitution gives

$$t_{C2} = 0.7 \times [2 + 6 \times 1.8]\, 10^{-15} \times 1.33 \times 10^{3} = 12 \text{ psec}$$

- The collector time delay of T9 and T3 including the wiring stray capacitances. For the X1.5 device, this time delay is

$$t_{d3} = (\ln 2)\underbrace{(16 \times 10^{3})}_{\substack{\text{Drain Resistance R3}}}[\underbrace{1.8 + 3.6}_{\substack{\text{One Gate-to-Drain and One Miller Cap}}} + 3.6 + \underbrace{10}_{\substack{\text{Stray}}}] \times 10^{-15} = 212 \text{ psec}$$

(Source follower cap of the following cell)

In the normal operating mode, all these time constants are settling together. Therefore, the overall time constant is the rss of all the time constants, and the overall time delay which is proportional to the time constant is also rss of all the time delays. Thus, the total basic cell time delay is

$$t_{d} = \sqrt{220^{2} + 12^{2} + 212^{2}} = 306 \text{ psec}$$

The X- and Y- inputs remain steady during the calculating cycle. Their delays do not affect the propagation of the sums and the carries through the chip and, therefore, do not affect the speed of the multiplication.

Another important parameter is the speed-power product of the logic gates used. Since nine gates are in the 576 μW basic cell, the equivalent gate power dissipation is $\frac{576}{9}$ = 64 μW. The longest delay path as calculated previously consists of two gate delays. Therefore, the net delay per gate is $\frac{306}{2}$ = 153 psec. The delay-power product of the differential current mode logic is then equal to

$$\text{Delay-power product} = 64\ \mu W \times 153 \text{ psec}$$

$$= 0.0098 \text{ pj}$$

16 x 16 Multiplier Performance

Based on the design and analytical data of the basic cell shown in the previous section, the 16 x 16 multiplier performance is summarized in Table 2. The following relations are used:

are also available in parallel format. The multiplier multiplies, shifts, and adds

*G McIver, et al "A Monolithic 16 x 16 Multiplier," ISSCC, Feb 74, p. 54, and U.S. Patent 3,900,724.



Table 2. 16 x 16 Multiplier Performance Summary

| Parameters | Performance | Units |
|---|---|---|
| Number of gates | 2400 | Gates |
| Chip size | 125 x 125 | mils |
| Multiplication rate | 102 | MHz |
| Throughput delay | 9.8 | nsec |
| Power dissipation | 148 | mW |
| Number of GaAs FET devices | 8340 | Devices |
| Equivalent gate delay-power product | 0.0098 | pj |
| Equivalent gate delay | 0.15 | nsec |

Total multiplier delay = 2 x 16 x (cell delay) = 32 td

Total multiplier power dissipation = 16 x 16 x (cell power dissipation)

Total multiplier chip edge = $\left(\sqrt{16 \times 16 \times (\text{cell area})}\right)$

Multiplication rate = 1/(32 td)

Total multiplier gates = 16 x 16 x (number of cell gates)

The multiplier achieves the speed goal of 100 MHz without resorting to pipelining which is considered a handicap in modern processing systems. Some processors cannot use pipelined multipliers at all. Some can use it but at the expense of extra circuits (and power) for delay compensations. In general, for the systems where feedback signal processing is required, the computed product must be available immediately for the succeeding computation and the excess clock delay of the pipelined multiplier is unacceptable. Examples where the pipelined multiplier cannot be used are:

- Recursive Digital filter
- Tracking loop
- Others requiring feedback processing.

The nonpipelined multiplier does not have these restrictions. The speed is achieved at the power level of less than 150 mm for the total 16 x 16 multiplier function.

times the word multiplication rate is required. If the word multiplication is set at



Summary and Conclusions

In this section, we presented several organizational concepts applicable to low power, high speed multiplier requirements. The all-parallel approach is selected because it has the highest potential to achieve a good speed/power ratio and requires development of only one circuit type. Among the all-parallel multiplication algorithms, the nonpipelined sequential-add algorithm is selected because it can be used in sign-magnitude as well as 2's complement numbering systems. It can also be used without restriction in any signal processing system, open-loop or feedback, recursive or non-recursive. TRW has proven the sequential-add algorithm and the desirability of current mode circuit topology through the successful application of bipolar silicon oxide-aligned-transistor (OAT) technology.

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